Next generation semiconductor devices and applications

(차세대 반도체 소자 및 응용)

장소: 공과대학 6호관 510호

시간: 화 (6-A, 6-B, 7-A, 7-B, 8-A, 8-B)

4. Principle of Semiconductor devices

4. Principle of Semiconductor devices

Classification of Semiconductor

Elemental semiconductors

: Composed of single species of atoms
: Si, Ge, Sn etc.

Intrinsic semiconductors

: Undoped semiconductor that does not contain impurity atoms or crystal defects
: # of electron = # of hole

Extrinsic semiconductors

: A semiconductor that contains impurities such as donors or acceptors and can control electrical conduction depending on the supplied electrons or holes.

- N-type : Pentavalent (As, Sb , donor) : Major carrier → electron
- P-type : Trivalent (In, Ga, acceptor) : Major carrier → hole

Compound Semiconductors

: Composed of two or more elemental compounds
: III-V compound (GaAs, GaP, InP, InAs, GaN etc.)
: II-VI compound (ZnO, CdS, ZnTe etc.)
: IV-VI compound (PbS) & IV-IV compound (SiC)

4. Principle of Semiconductor devices

Intrinsic Semiconductor

TABLE 12-2
A Summary of Band-Gap Energies for Semiconducting Materials

General Type	Material	Band Gap (eV)
IV	Si	1.1
	Ge	0.68
	AlSb	2.4
	GaAs	1.4
	GaSb	0.67
	InP	1.25
	InAs	0.33
	InSb	0.18
II-VI	ZnTe	2.1
	CdSe	1.7
	CdTe	1.5
	CdS	2.4
	HgSe	0.6

- Organic semiconductor
- Metal Oxide Semiconductor
- 2D semiconductor

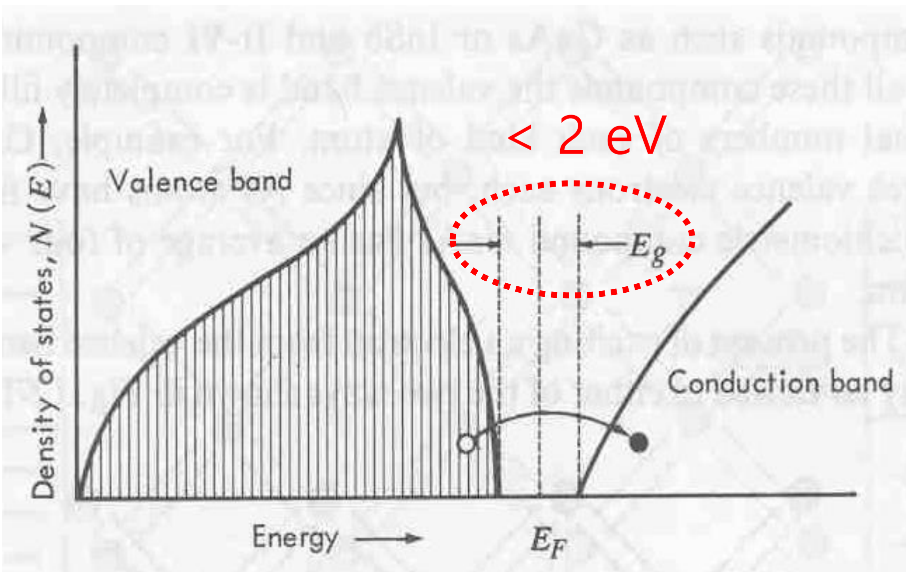
$1\ eV < E_g < 2\ eV$

- **Pure elements: Si, Ge**
- **Stoichiometric compound: GaAs, CdS**

4. Principle of Semiconductor devices

Intrinsic Semiconductor

Band structure of semiconductor



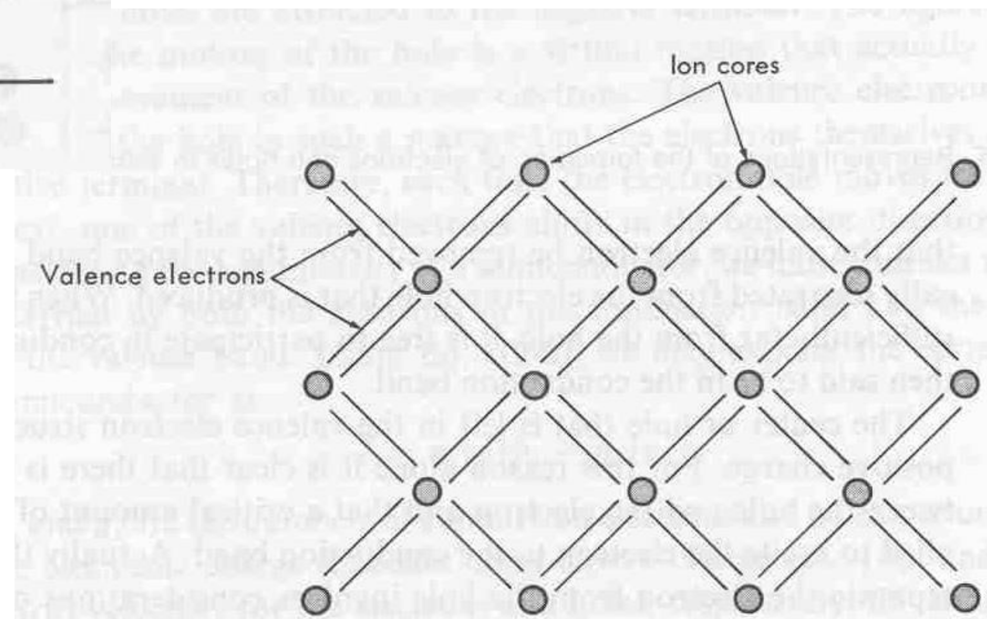
[Intrinsic semiconductor]

Valence electron : 4

G.14 : Si, Ge

Average valence electron : 4

III-V: GaAs, InSb
II-VI: CdSe, ZnS

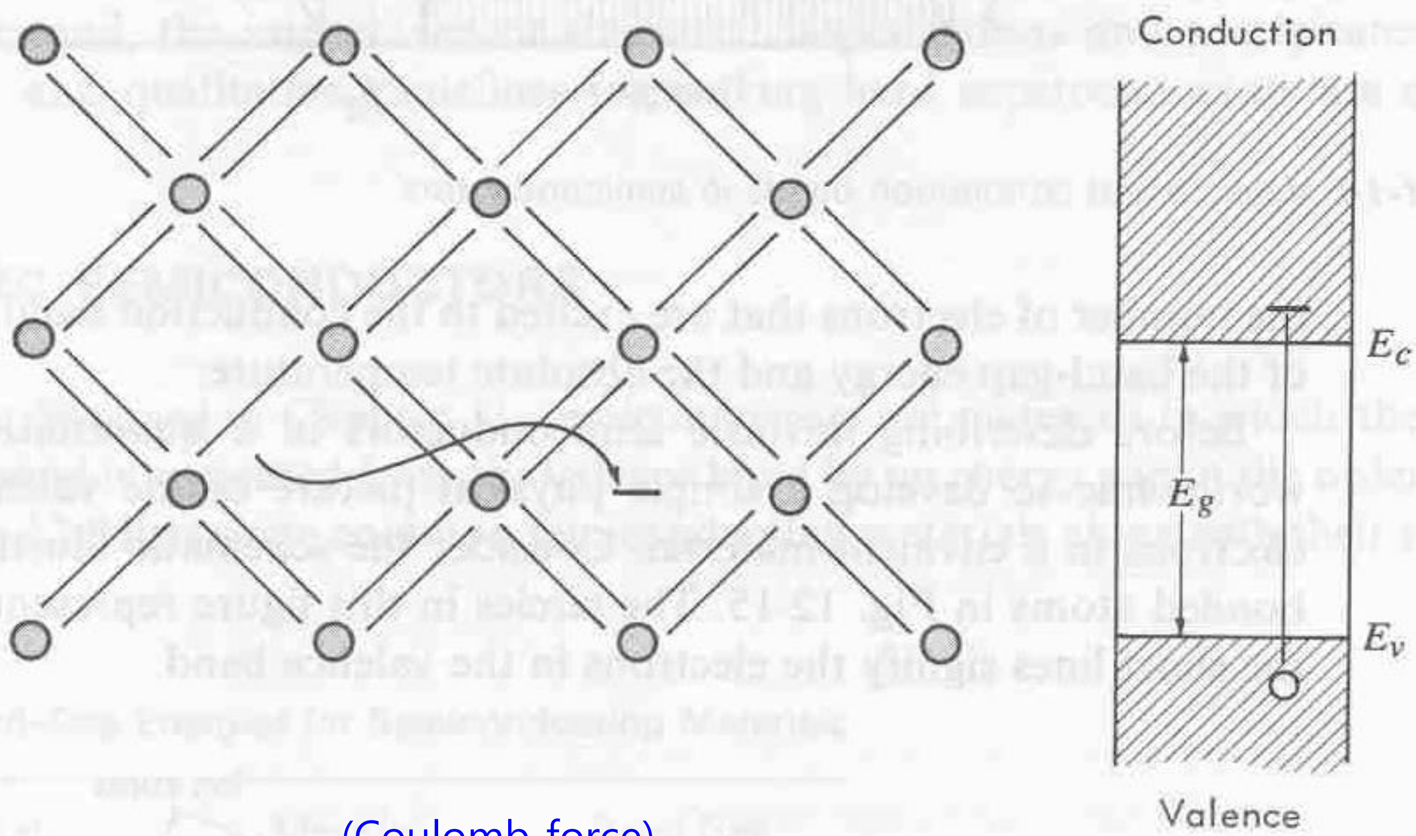


Covalent bond structure of Si

4. Principle of Semiconductor devices

Intrinsic Semiconductor

- Energy band gap(E_g) and Formation of electron-hole pair



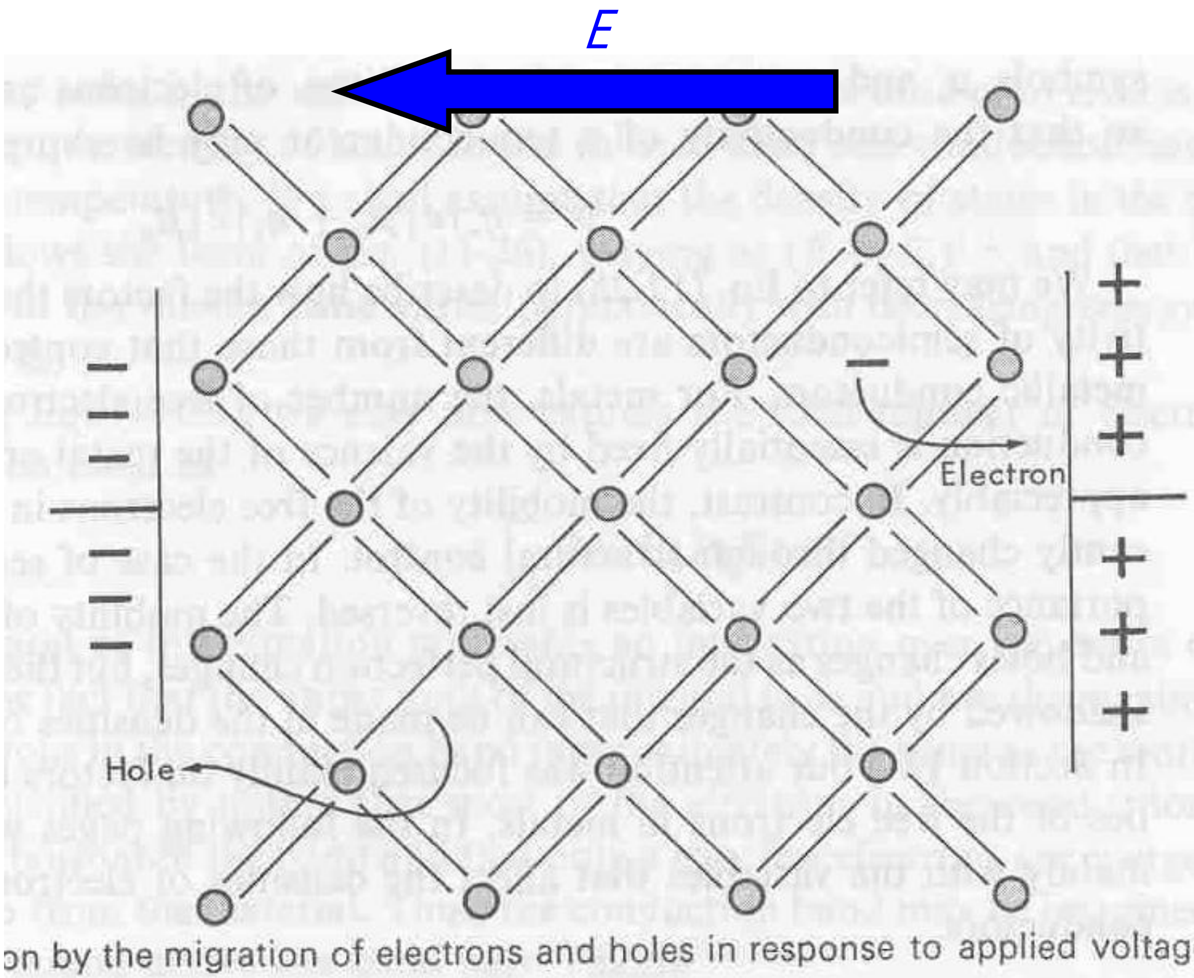
(Coulomb force)

FIG. 12-16 Representations of the formation of electrons and holes in semiconductors

4. Principle of Semiconductor devices

Intrinsic Semiconductor

: Electric conduction in intrinsic semiconductor



Electric field (←)

Net direction of elec. (→)

Net direction of hole (←)

Current direction (←)

Conduction of Semiconductor migration of i) electrons in the conduction band
ii) holes in the valence band

4. Principle of Semiconductor devices

The formula for electrical conduction in intrinsic semiconductors

$J = \eta_e|e|v_e$ *at conductor*

J = current density

η (ita) = number of conduction elec. per unit vol.

$$J = \eta_e|e|v_e + \eta_h|e|v_h$$

$J = \sigma E$

$\sigma = J / E$

$$\sigma = \eta_e|e|\left(\frac{v_e}{E}\right) + \eta_h|e|\left(\frac{v_h}{E}\right)$$

Mobility (이동도)

$$\sigma = \eta_e|e|\mu_e + \eta_h|e|\mu_h$$

Factors affecting the conductivity of semiconductors.

: mobility, # of conduction elec. & hole per unit vol.

of elec. & hole

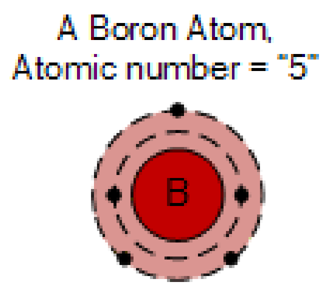
4. Principle of Semiconductor devices

Extrinsic Semiconductor

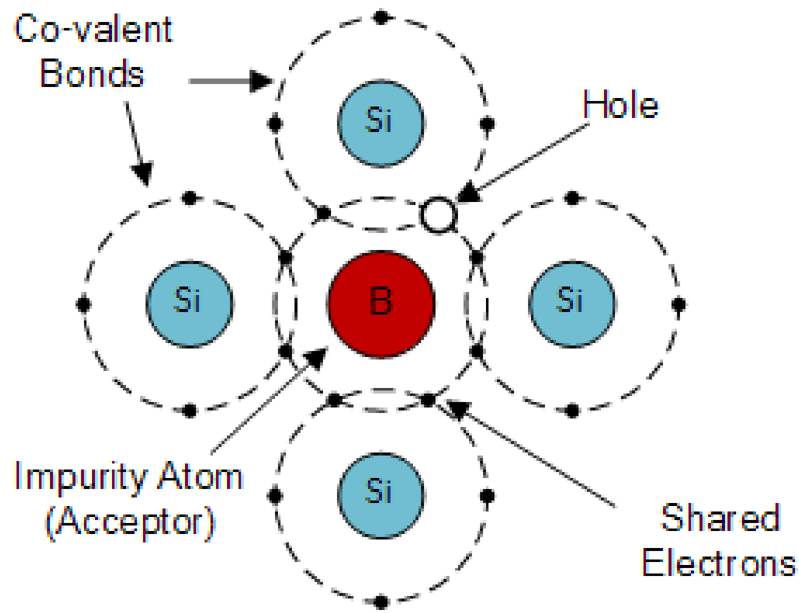
Doping

: Hole?

- The absence of an electron in a particular place in an atom.
- Virtual particle, Not a physical particle.
- Move through the lattice as electrons can.



Boron atom showing 3 electrons in its outer valence shell (L)



P-Type Semiconductor

*The doped semiconductor is always neutral

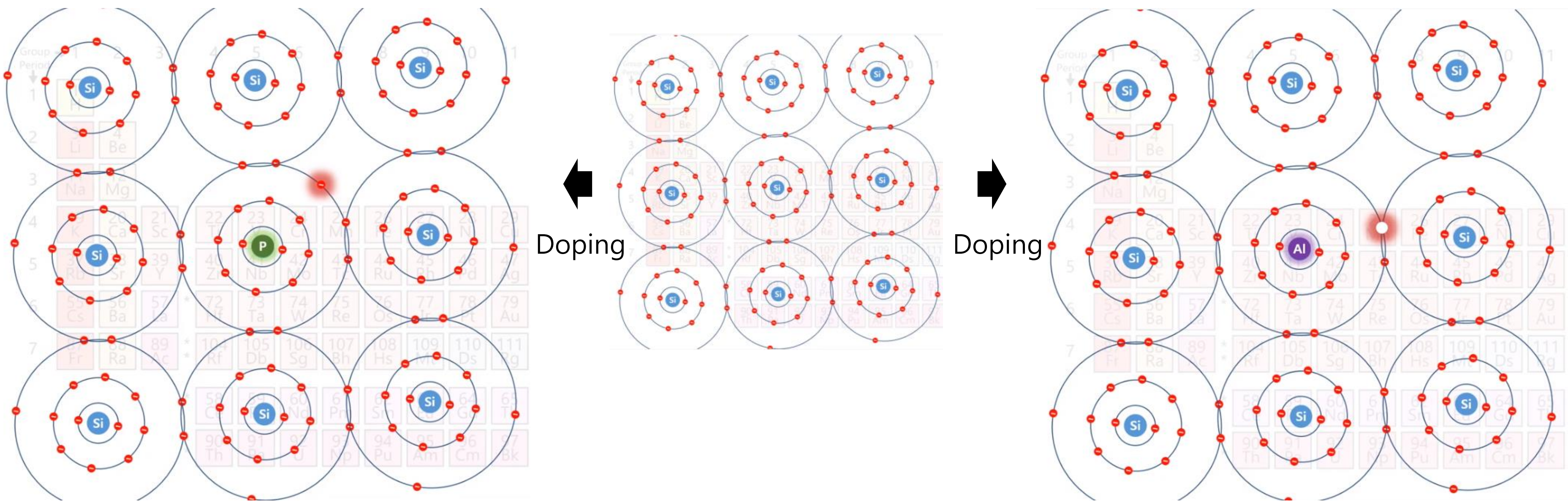
4. Principle of Semiconductor devices

Extrinsic Semiconductor

→ Can control electrical conduction according to supplied electrons(donors) or holes(acceptors)
→ 5 group (donor) : n-type , 3 group (acceptor) : p-type

(a) n-type semiconductor

(b) p-type semiconductor



Group V: P, As, Sb,..
Major carrier → electron

Group III: B, Al, Ga, In,..
Major carrier → hole

4. Principle of Semiconductor devices

Extrinsic Semiconductor

Position of donor & acceptor level

Energy level of donor & acceptor

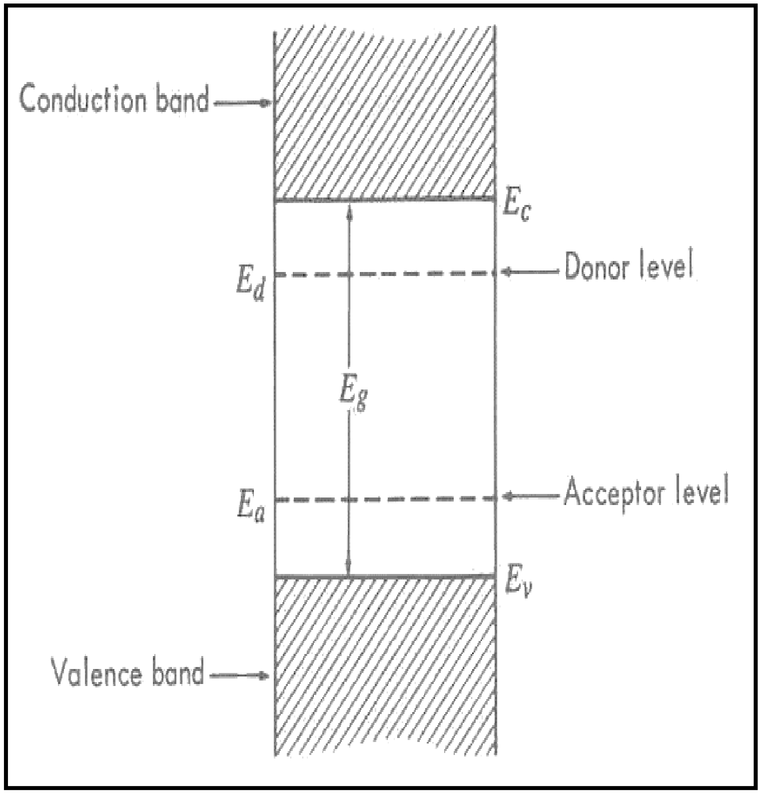
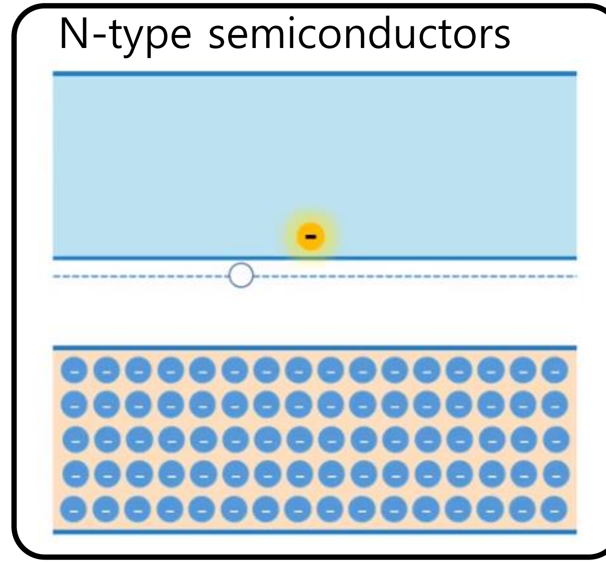
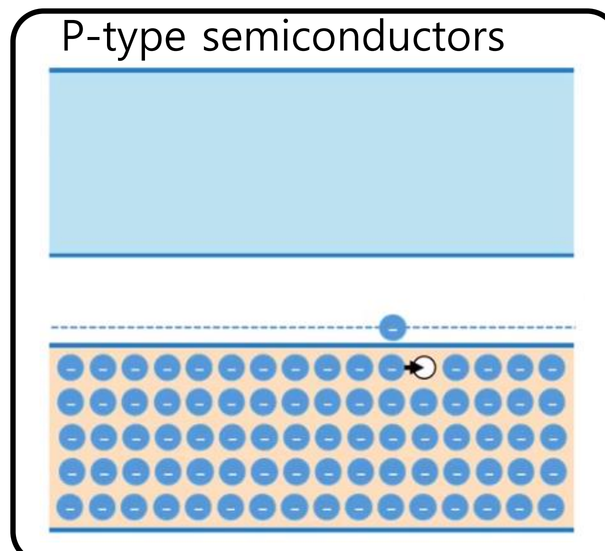


Fig. 3-19 Donor and acceptor energy levels in semiconductors





4. Principle of Semiconductor devices

Extrinsic Semiconductor

Position of donor & acceptor level

*kT_{300K} = 0.0259 eV

Energy level of donor & acceptor

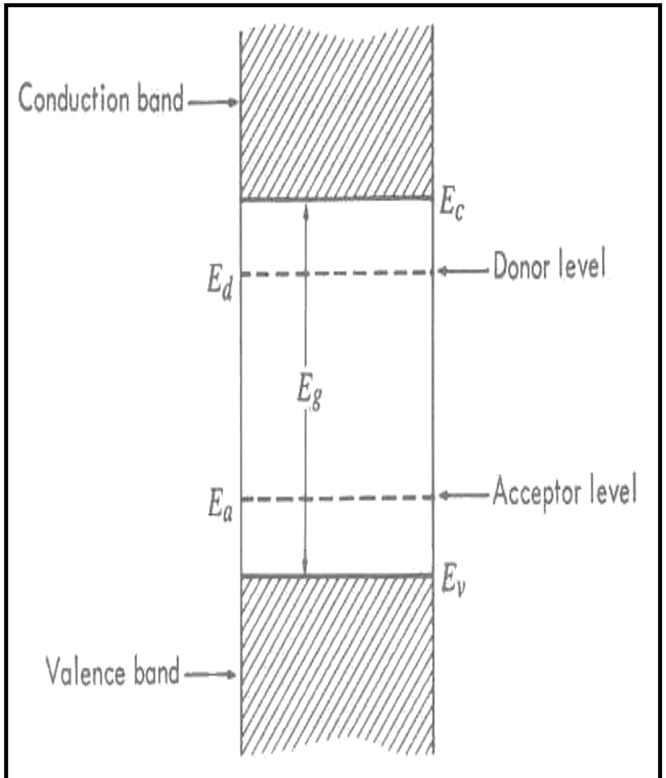


Fig. 3-19 Donor and acceptor energy levels in semiconductors

Si : Energy level of donor & acceptor

Donor Impurities		Acceptor Impurities	
Impurity	$E_c - E_d$ (eV)	Impurity	$E_a - E_v$ (eV)
P	0.044	B	0.045
As	0.049	Al	0.057
Sb	0.039	Ga	0.067
Li	0.033	In	0.16

Ge : Energy level of donor & acceptor

Donor Impurities		Acceptor Impurities	
Impurity	$E_c - E_d$ (eV)	Impurity	$E_a - E_v$ (eV)
Li	0.0093	Zn	0.029
P	0.012	B	0.0104
As	0.0127	Al	0.0102
Sb	0.0097	Ga	0.0108
Bi	0.012	In	0.0112
		Cu	0.040

4. Principle of Semiconductor devices

Temp. dependence of carrier concentrations in Extrinsic semiconductor

In case, Si, dopant: As atoms (2 x 10^{21}) -> n-type Si

☐ **Temp. dependence of Fermi energy**

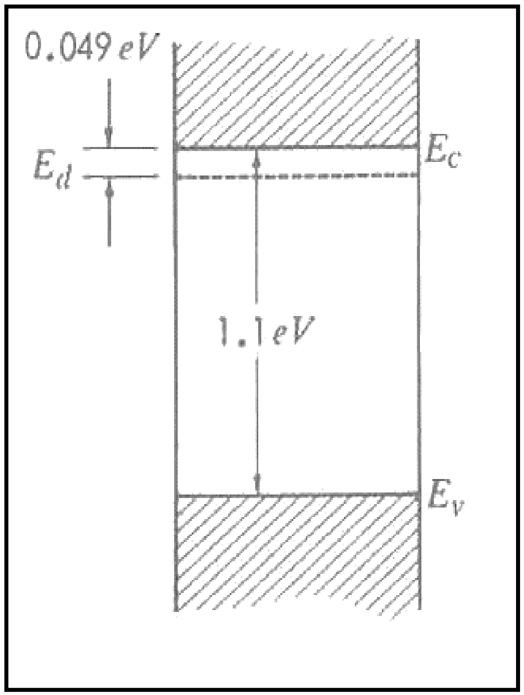
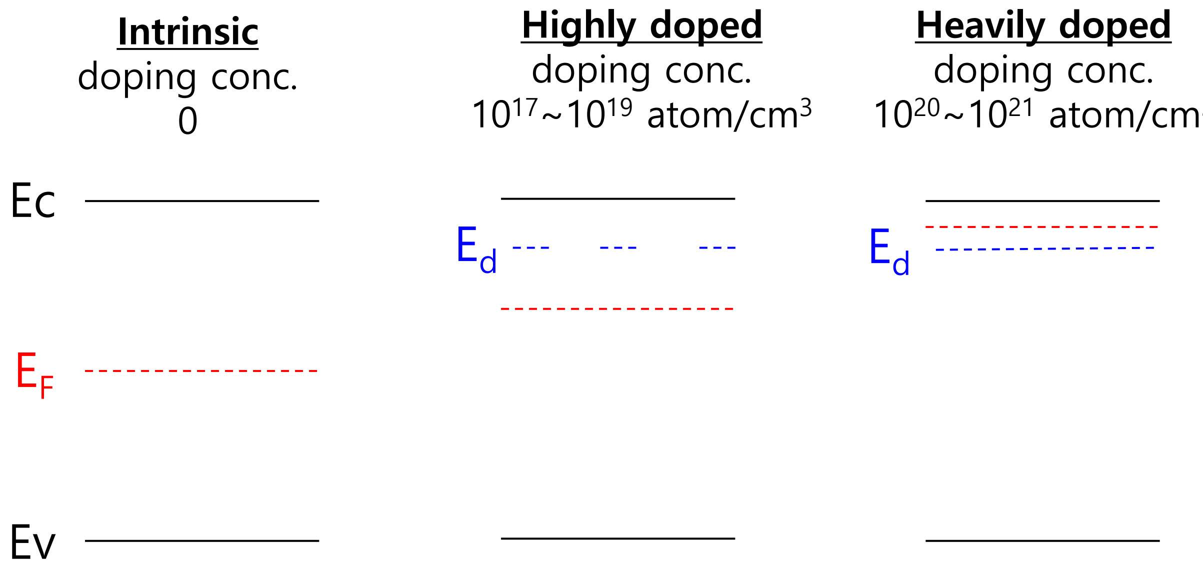


Fig. 3-20 Energy levels in an n-type semiconductor and dependence of the Fermi energy on temperature



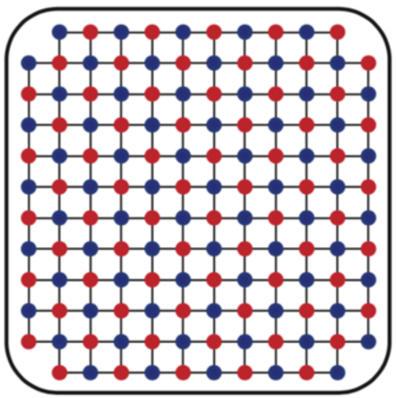
The factors that affect to the Fermi energy level

i) Doping concentration
ii) Absolute temperature

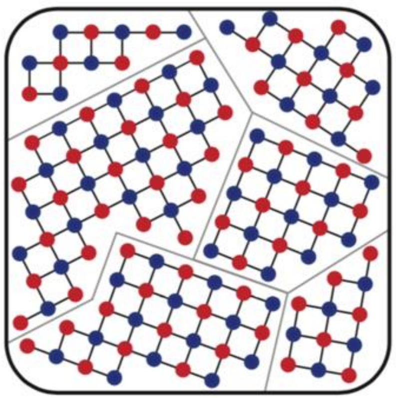
4. Principle of Semiconductor devices

Crystallinity of Silicon

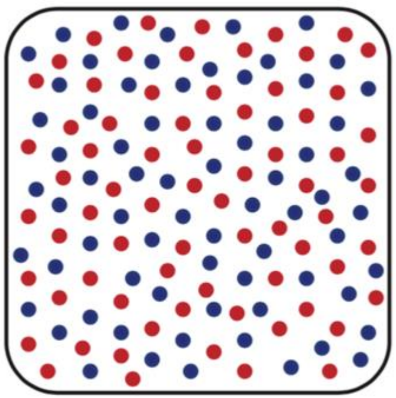
Single crystal



Polycrystalline



Amorphous



Mobility	High 600 cm^2/Vs	Moderate (~100 cm^2/Vs)	Low (1 ~ 10 cm^2/Vs)
Resistance	Low	Moderate	High
Process difficulty	High	Moderate	Low

4. Principle of Semiconductor devices

Metal-Metal junction

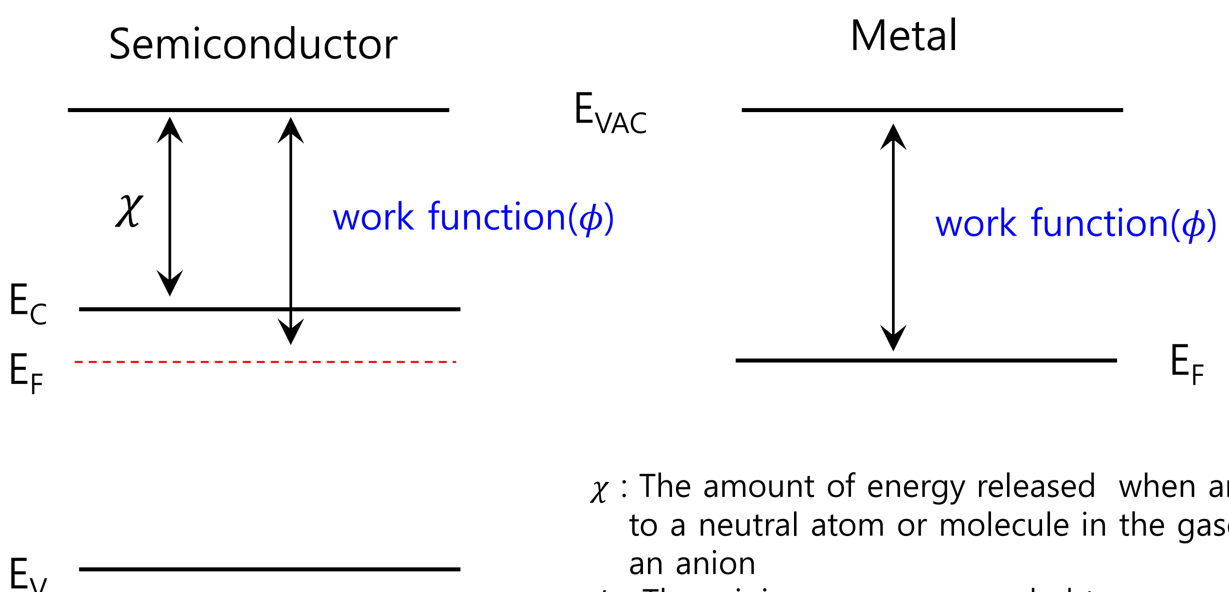
2-1. Property of Metal

i) Energy bandgap = 0 eV

ii) Can be regarded as N++ or P++ semiconductors

iii) Excess carriers inside metals: L_{diff} = 0, lifetime = 0

- No excess carriers (δn & δp = 0)
- Instant decay or recombination of excess carriers



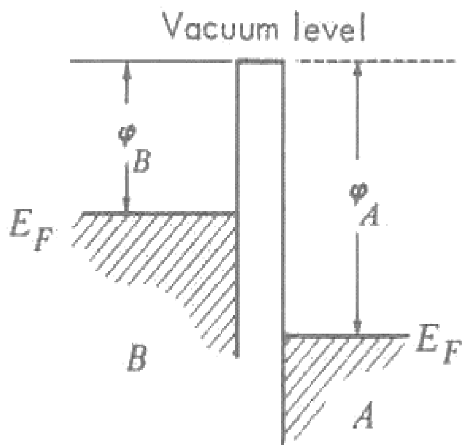
χ : The amount of energy released when an electron attaches to a neutral atom or molecule in the gaseous state to form an anion

ϕ : The minimum energy needed to remove an electron from a solid to a point in the vacuum immediately outside the solid surface.

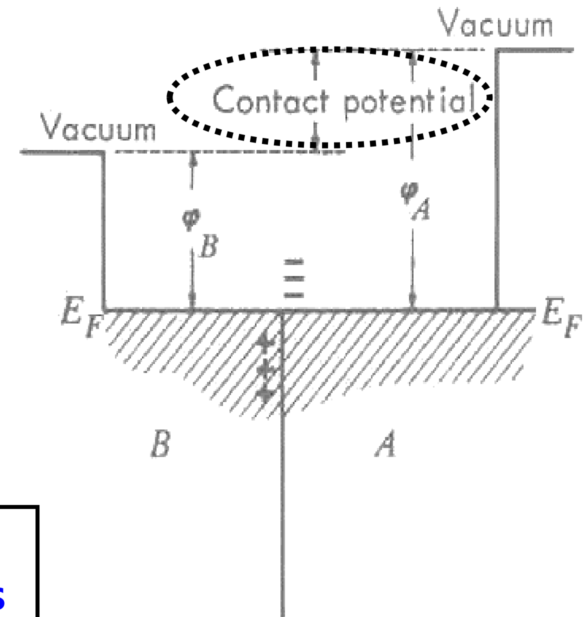
4. Principle of Semiconductor devices

Metal-Metal junction

: The electron flow from a metal with a small work function to a metal with large work function



(a) Before contact



(b) After contact

❖ **Work function(ϕ) : vacuum level – Fermi energy**
❖ **Contact potential = Difference between Work Functions**

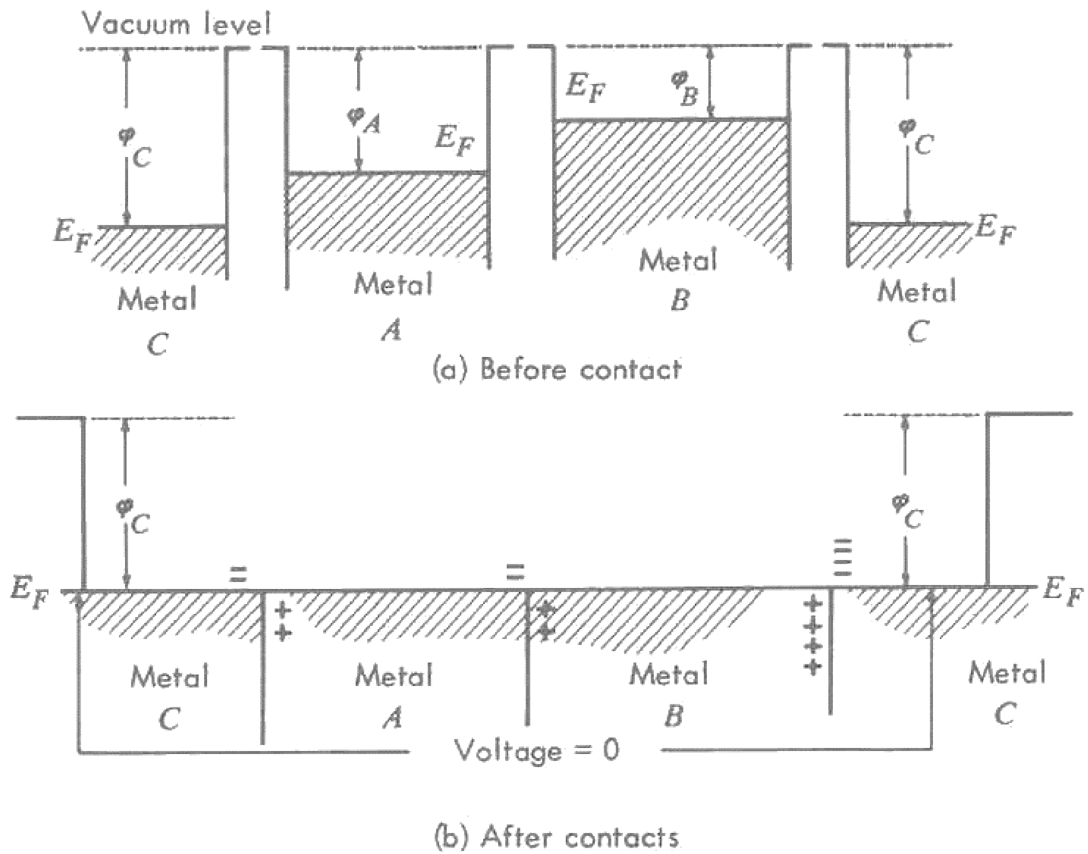
→ **Fermi energy constant.**

※ Tip to drawing the band diagram of Junction
- Align the E_F
- In case of Metal, " No " band bending
- In case of Semiconductor, bend bending

4. Principle of Semiconductor devices

Metal-Metal junction

: Contact potential



$(\phi_C - \phi_A)+(\phi_A - \phi_B)+(\phi_B - \phi_C)=0$

Contact voltages produced by contacting metals A and B with lead wire C.
The voltage between the two ends of the lead wire is zero.

4. Principle of Semiconductor devices

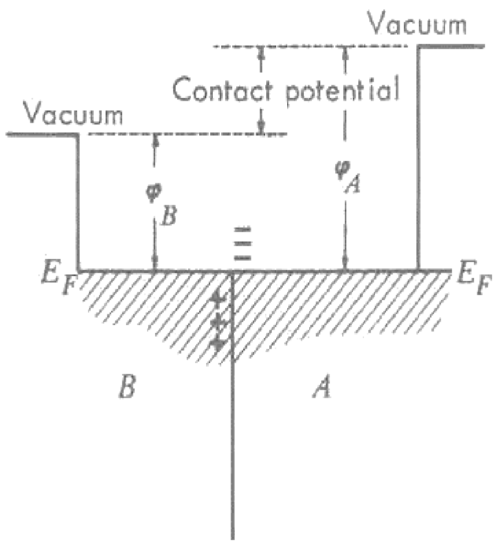
Metal-Metal junction

2-2. Electrical property of metal-metal contact

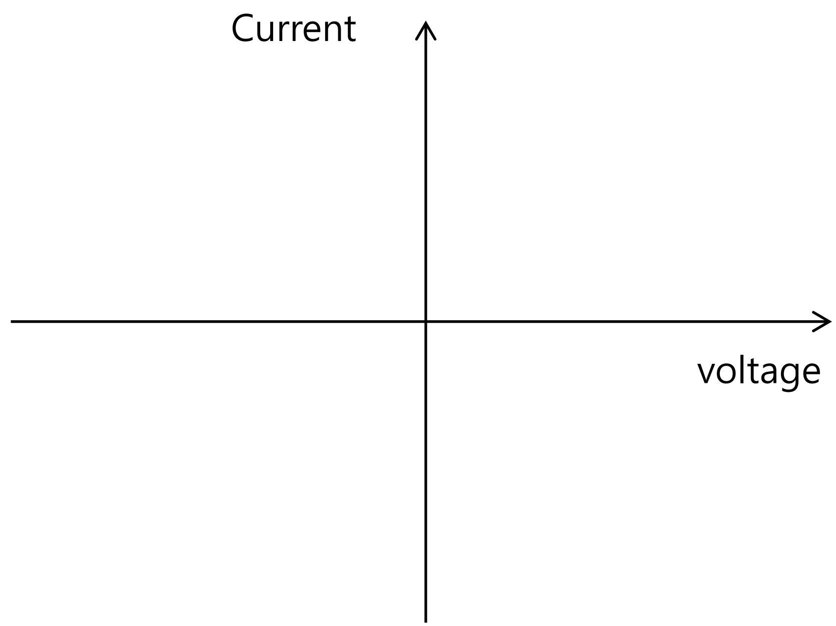
: **Ohmic contact**

> a junction between two conductors that has a **linear current–voltage (I-V) curve** as with Ohm's law.

> **V = IR**



(b) After contact



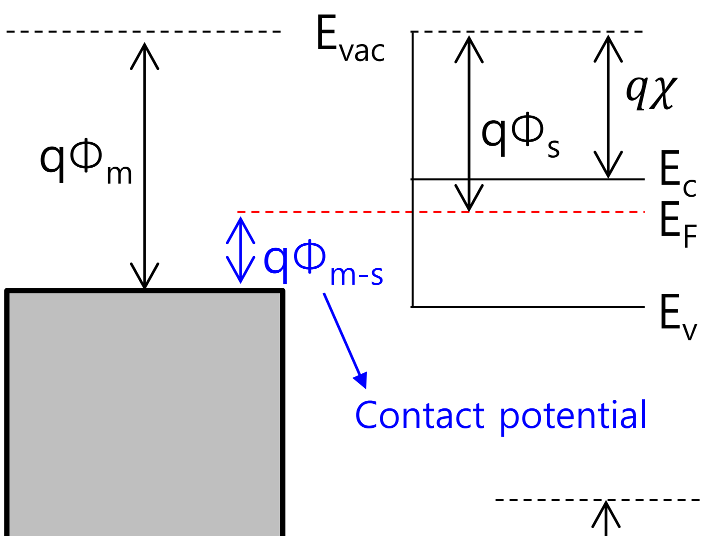
4. Principle of Semiconductor devices

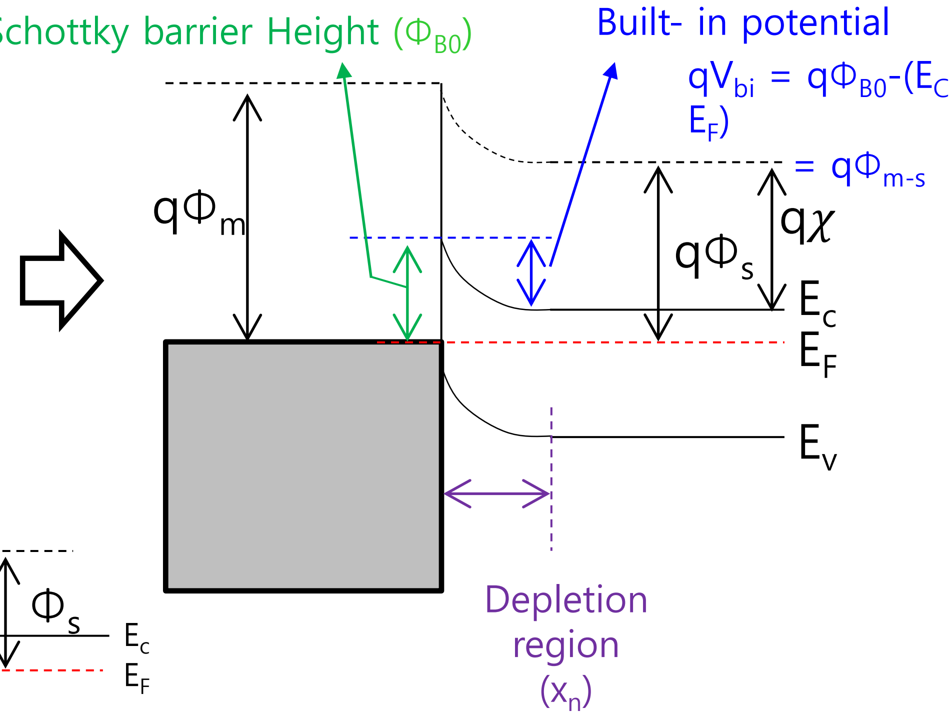
Metal-Semiconductor junction

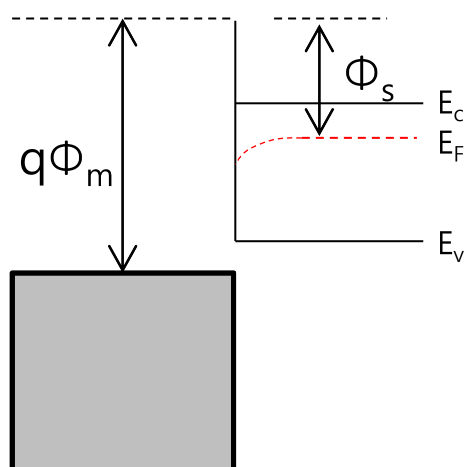
: Ohmic or Schottky contact depend on relative work function

$$q\chi = q\Phi_s - (E_C - E_F)$$

3-1. Contact between metal and **n-type** semiconductor ($\Phi_m > \Phi_s$)







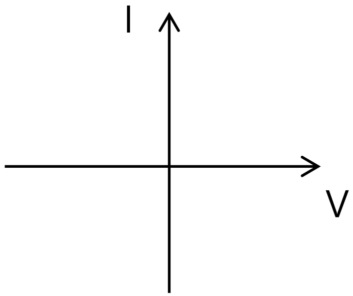
Φ at metal
χ at semiconductor
> the eigenvalue of material

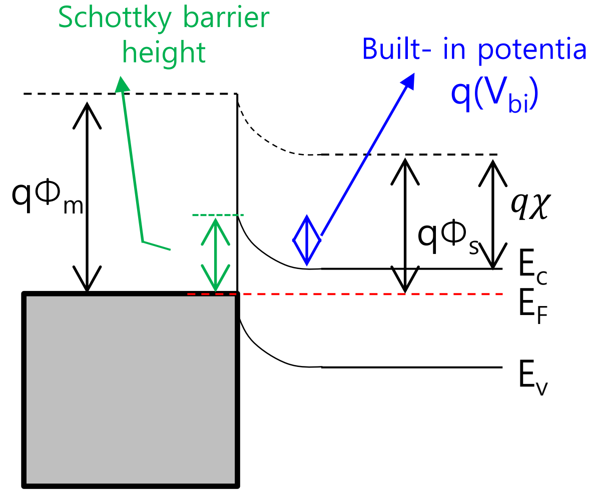
4. Principle of Semiconductor devices

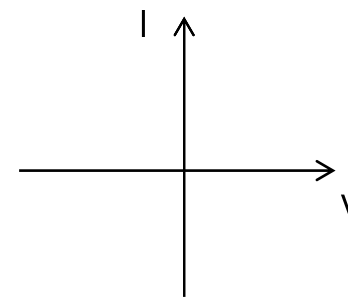
Metal-Semiconductor junction

3-1. Contact between metal and **n-type** semiconductor ($\Phi_m > \Phi_s$)

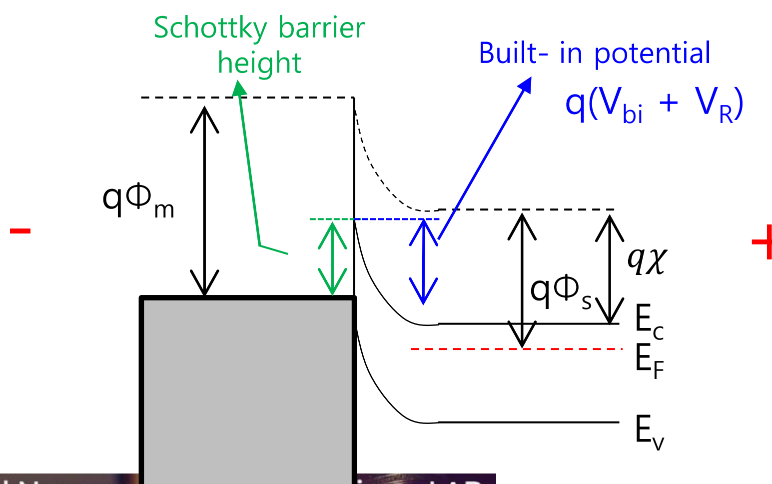
※ Tip
+ potential : Band ↓
- potential : Band ↑



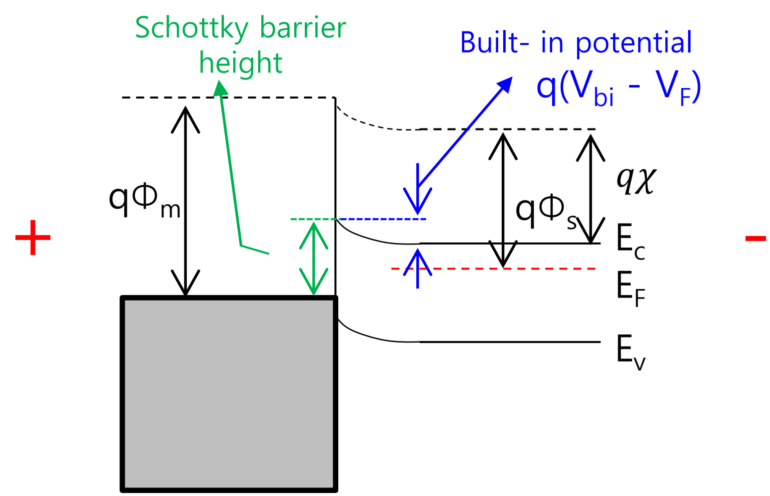




- Reverse bias



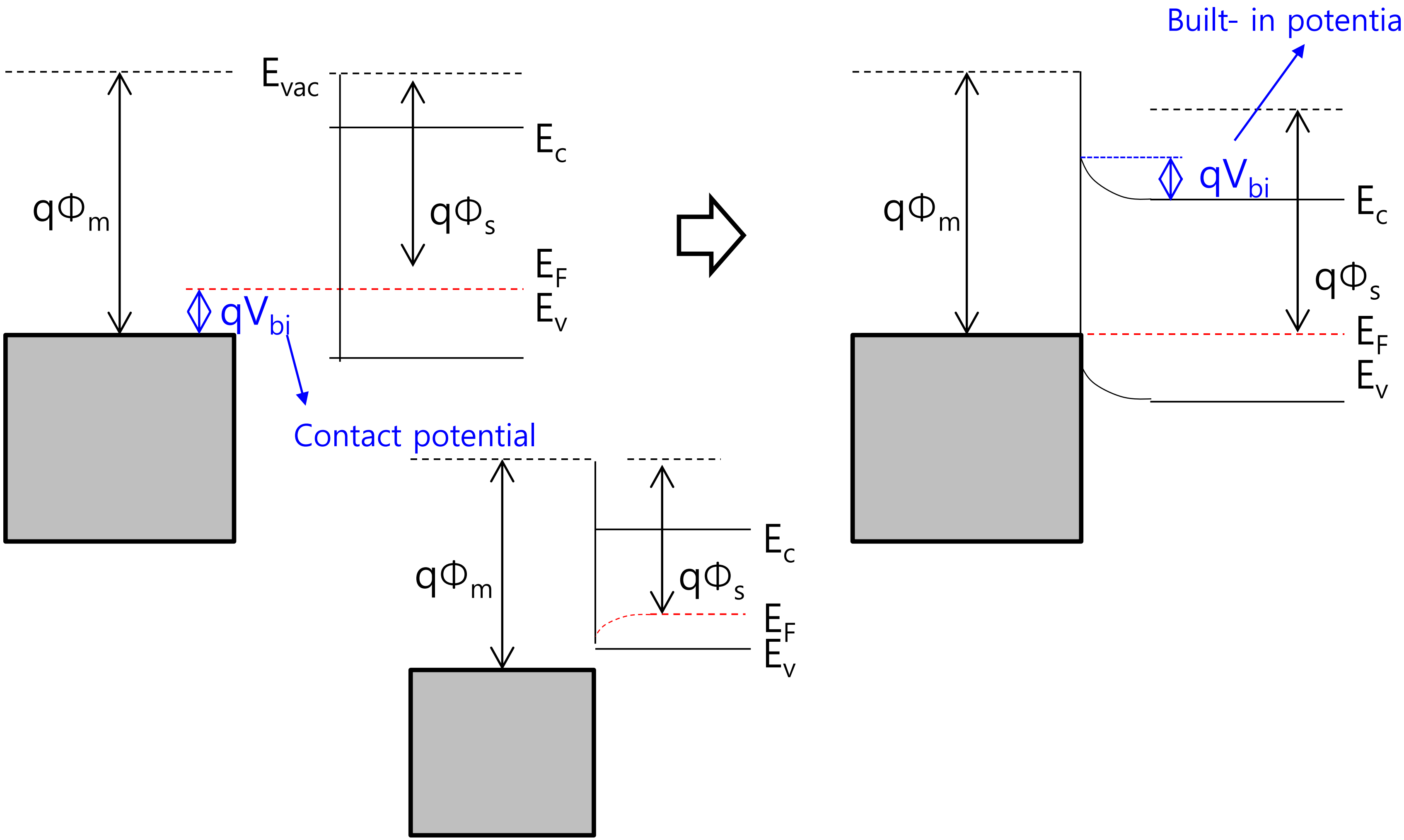
- Forward bias



4. Principle of Semiconductor devices

Metal-Semiconductor junction

3-2. Contact between metal and **p-type** semiconductor ($\Phi_m > \Phi_s$)

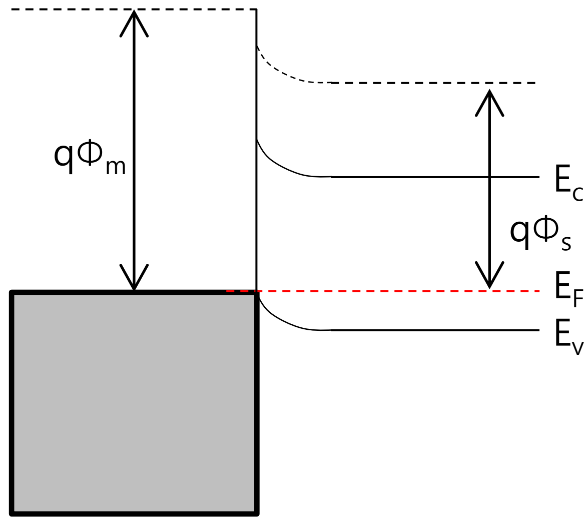


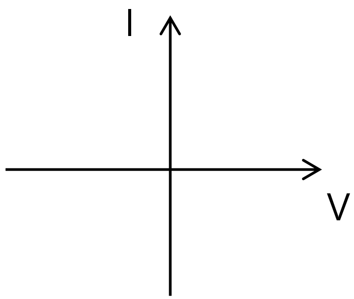
4. Principle of Semiconductor devices

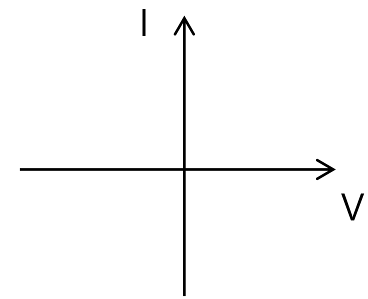
Metal-Semiconductor junction

3-2. Contact between metal and **p-type** semiconductor ($\Phi_m > \Phi_s$)

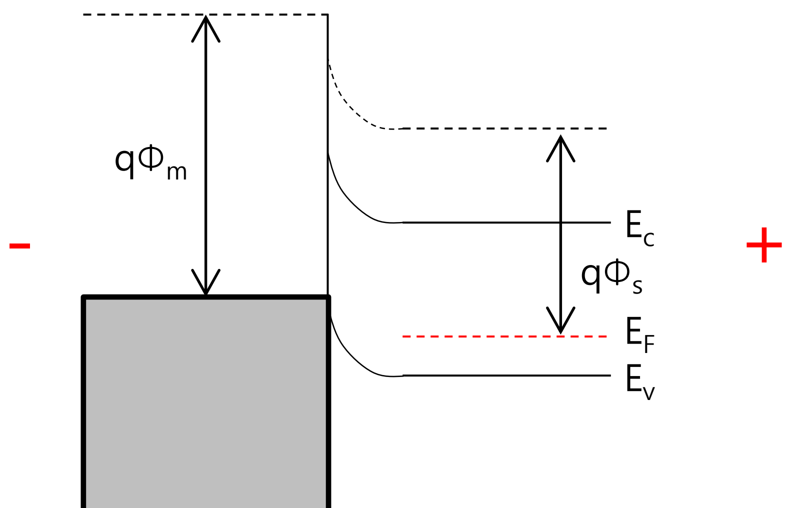
※ Tip
+ potential : Band ↓
- potential : Band ↑



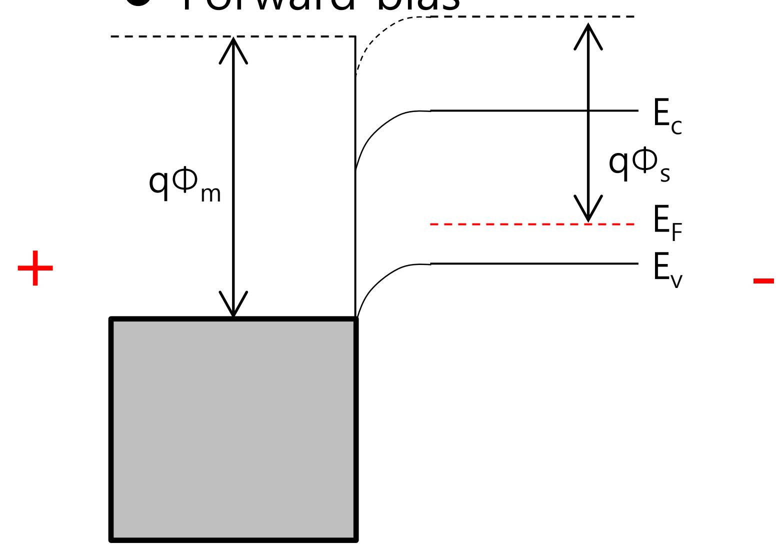




- Reverse bias



- Forward bias

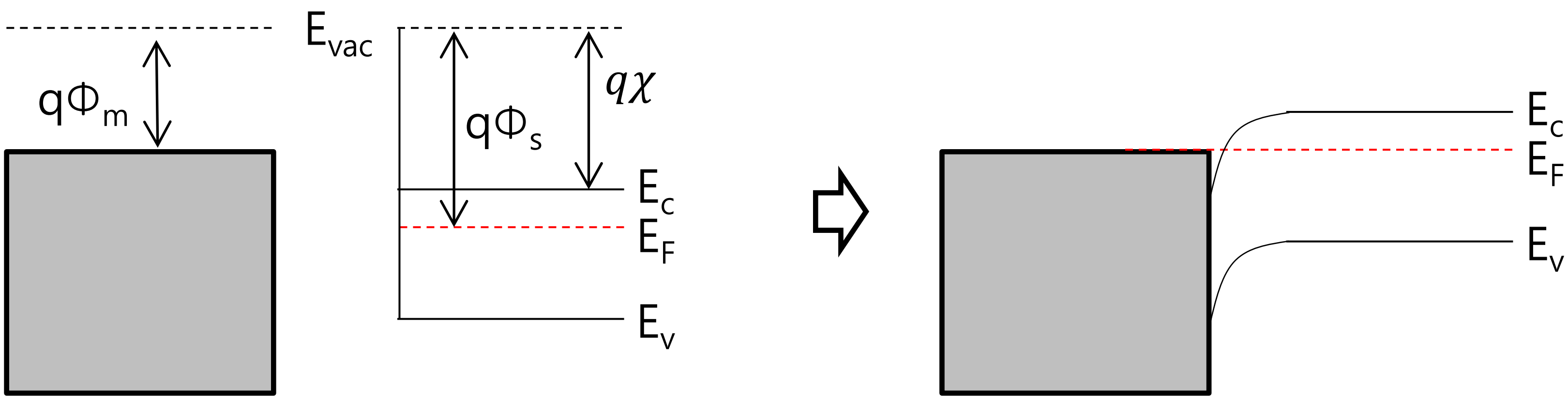


4. Principle of Semiconductor devices

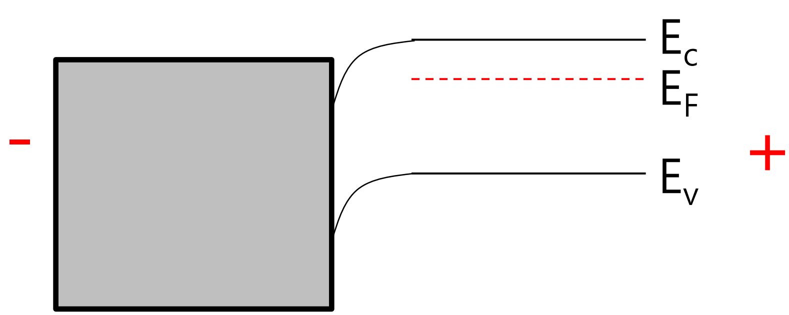
Metal-Semiconductor junction

3-2. Contact between metal and **n-type** semiconductor ($\Phi_m < \Phi_s$)

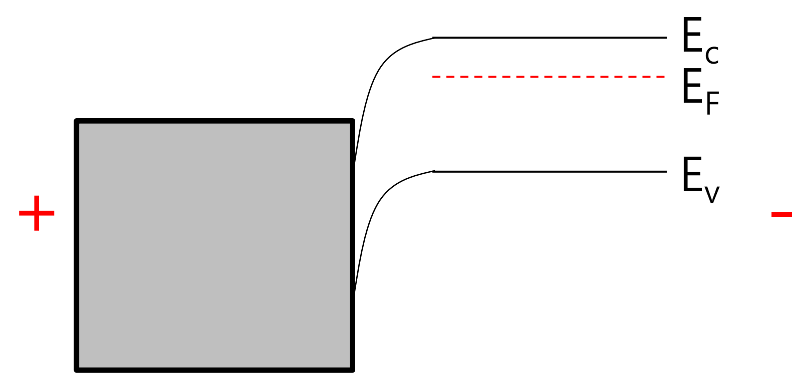
※ Tip
+ potential : Band ↓
- potential : Band ↑



- Reverse bias



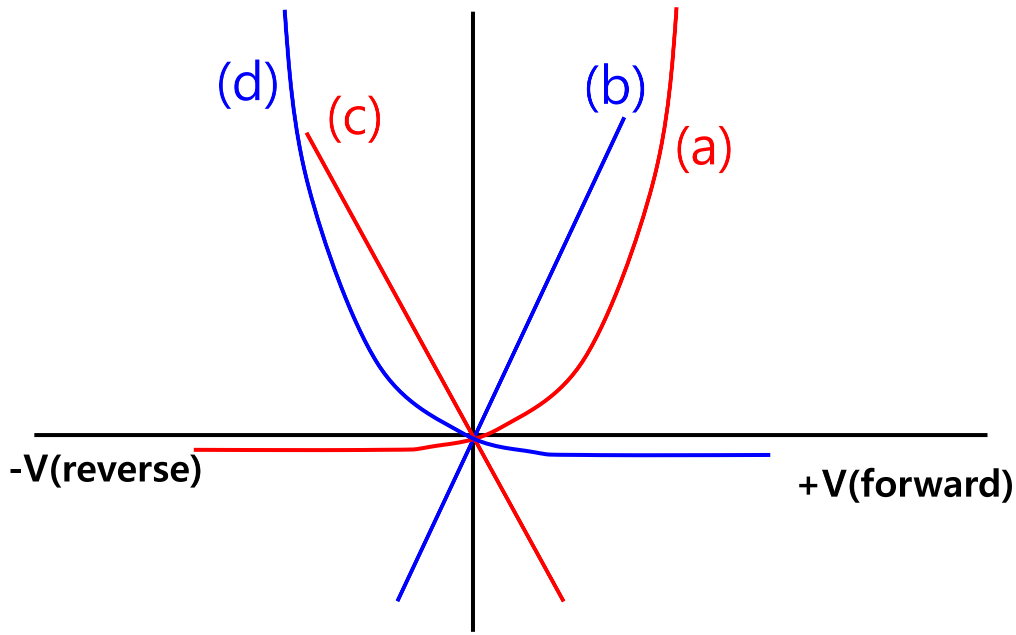
- Forward bias



4. Principle of Semiconductor devices

Metal-Semiconductor junction

3-3. Summary of contact property of Metal-Semiconductor

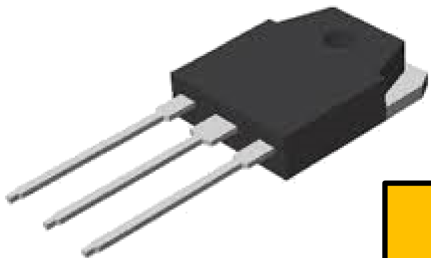


(a) $\phi_m > \phi_s$ (n-type semiconductor): rectifying
(b) $\phi_m < \phi_s$ (n-type semiconductor): Ohmic
} n-type

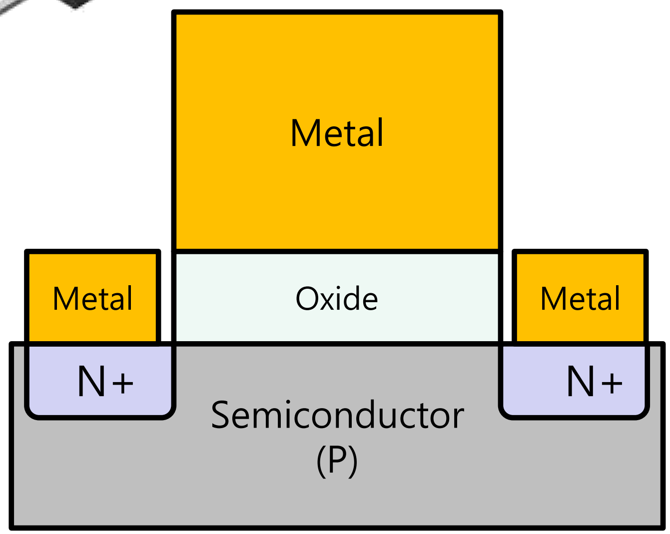
(c) $\phi_m > \phi_s$ (p-type semiconductor): Ohmic
(d) $\phi_m < \phi_s$ (p-type semiconductor): rectifying
} p-type

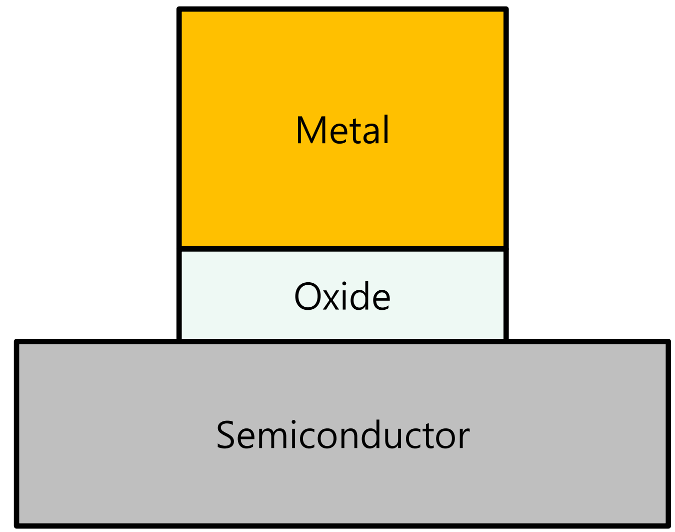
4. Principle of Semiconductor devices

Metal-Oxide-Semiconductor



MOSFET vs. MOS





MOS = Metal – oxide – Semiconductor

To understand the operation of MOSFET, we need to learn about MOS structure!

Homework What is the difference between MOSFET and TFT?

Channel: Organic, Oxide, 2D, Perovskite

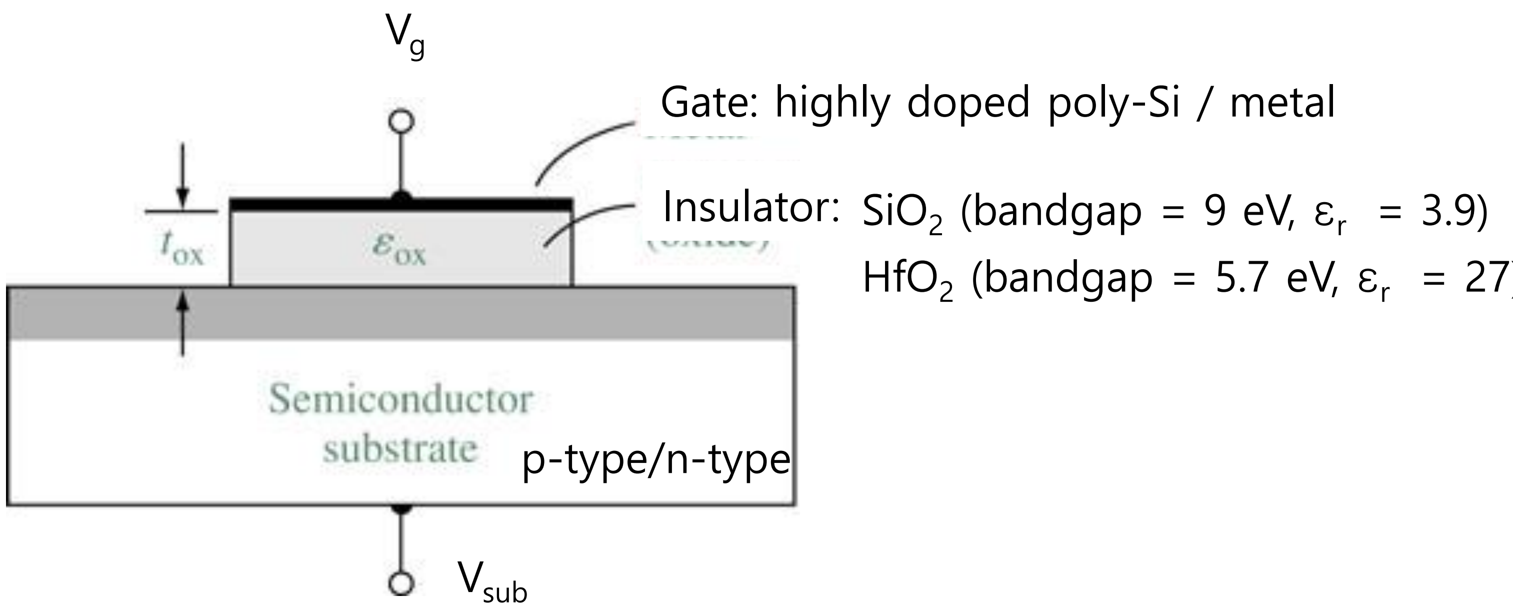
4. Principle of Semiconductor devices

Metal-Oxide-Semiconductor

1. Concept

: MOS capacitor structure

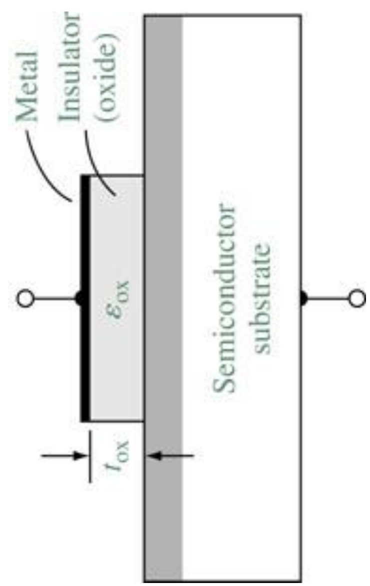
: 2-terminal



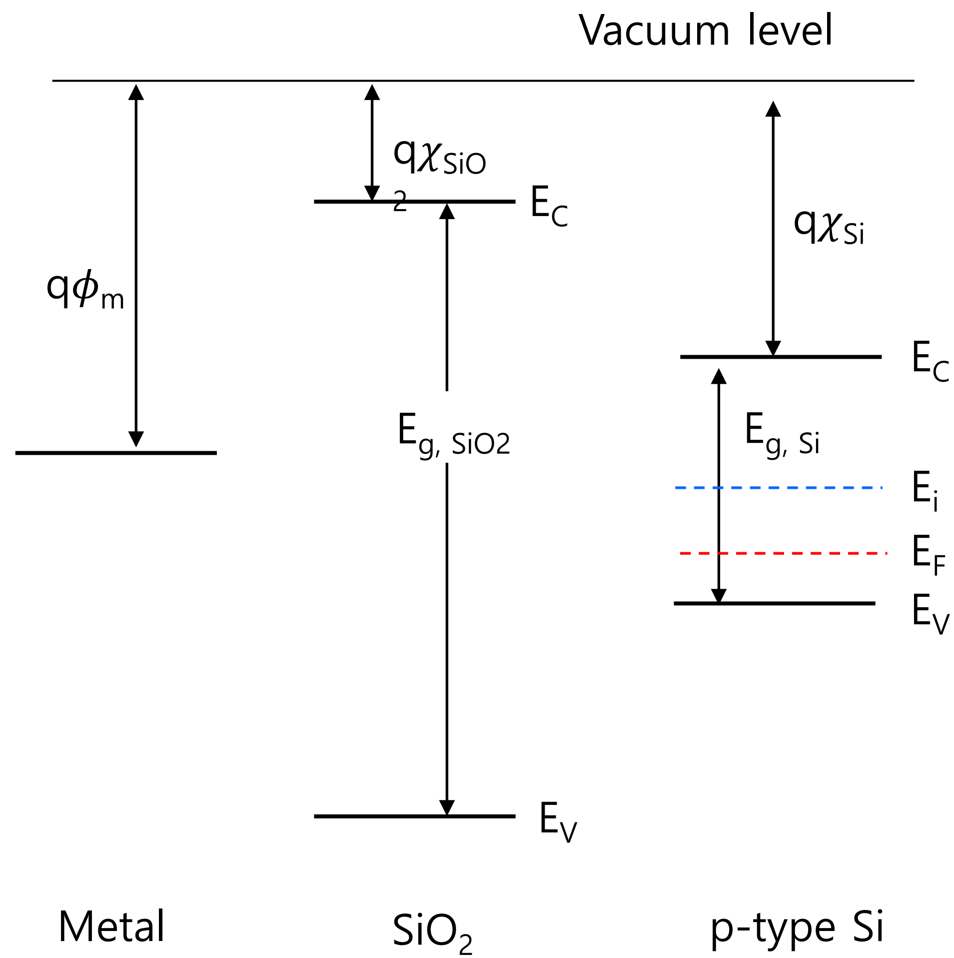
4. Principle of Semiconductor devices

Metal-Oxide-Semiconductor

1. Concept
: MOS capacitor structure
: 2-terminal



- **When, $\phi_m < \phi_{Si}$**



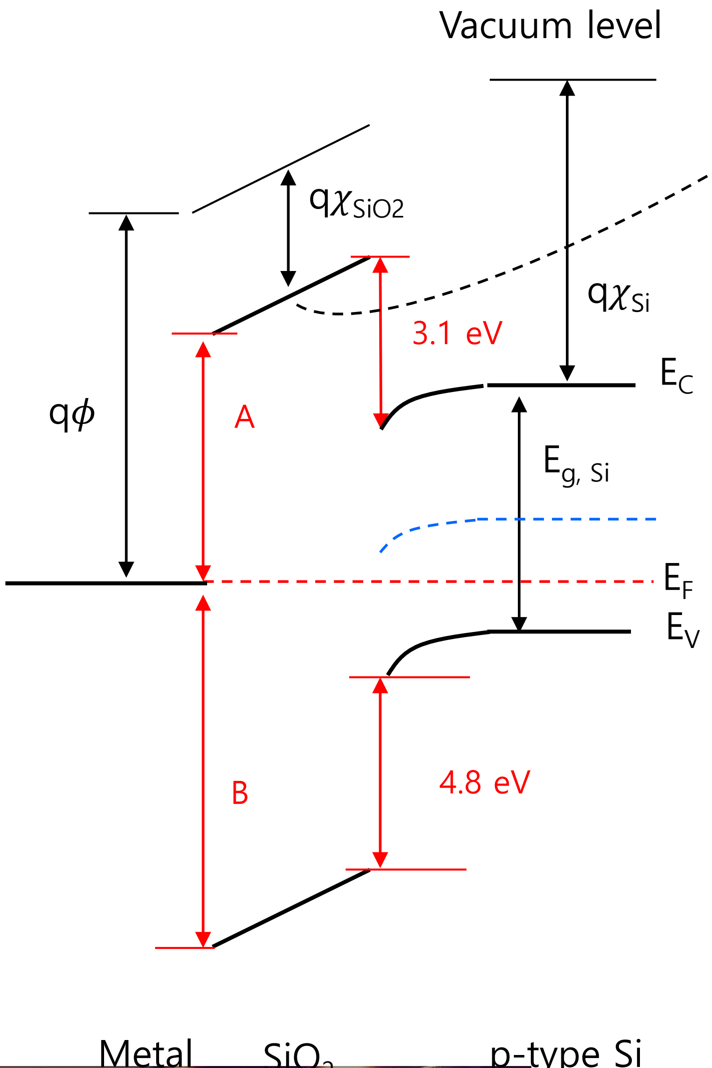
4. Principle of Semiconductor devices

Metal-Oxide-Semiconductor

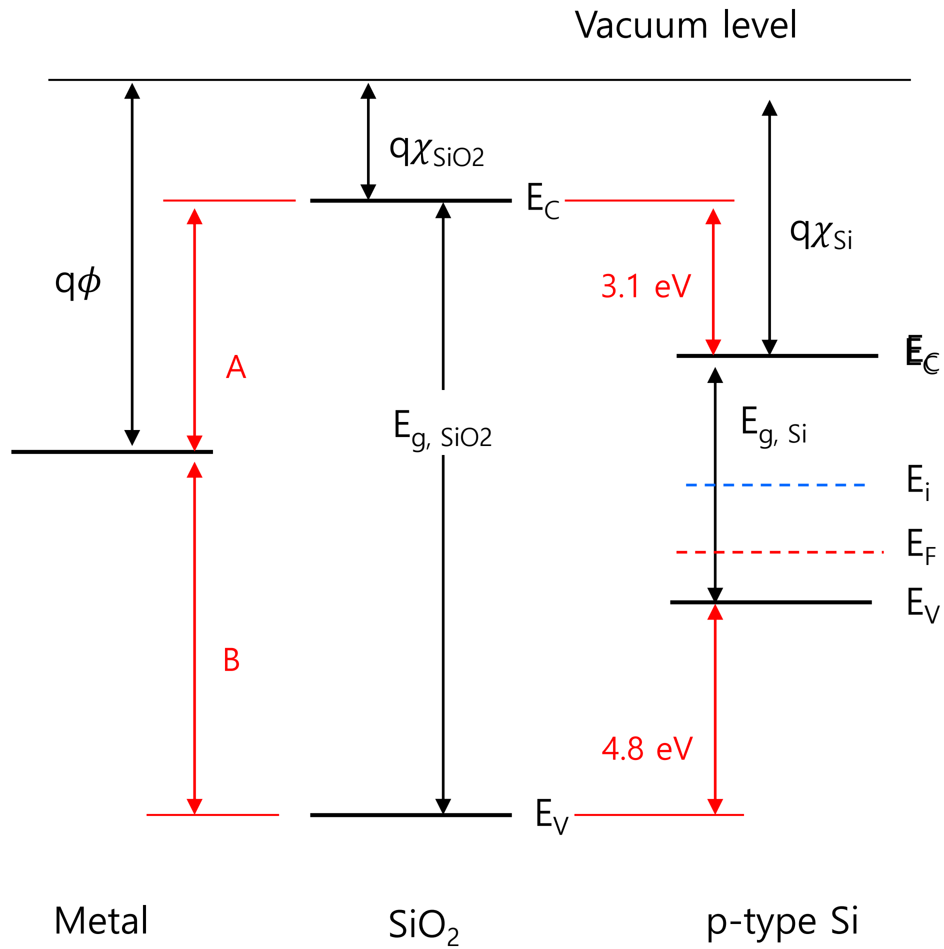
1. Concept

: MOS capacitor structure

ρ in oxide = 0 → dE/dx = 0 → E is constant
: bend bending of the oxide is linear



▪ **When, $\phi_m < \phi_{Si}$**

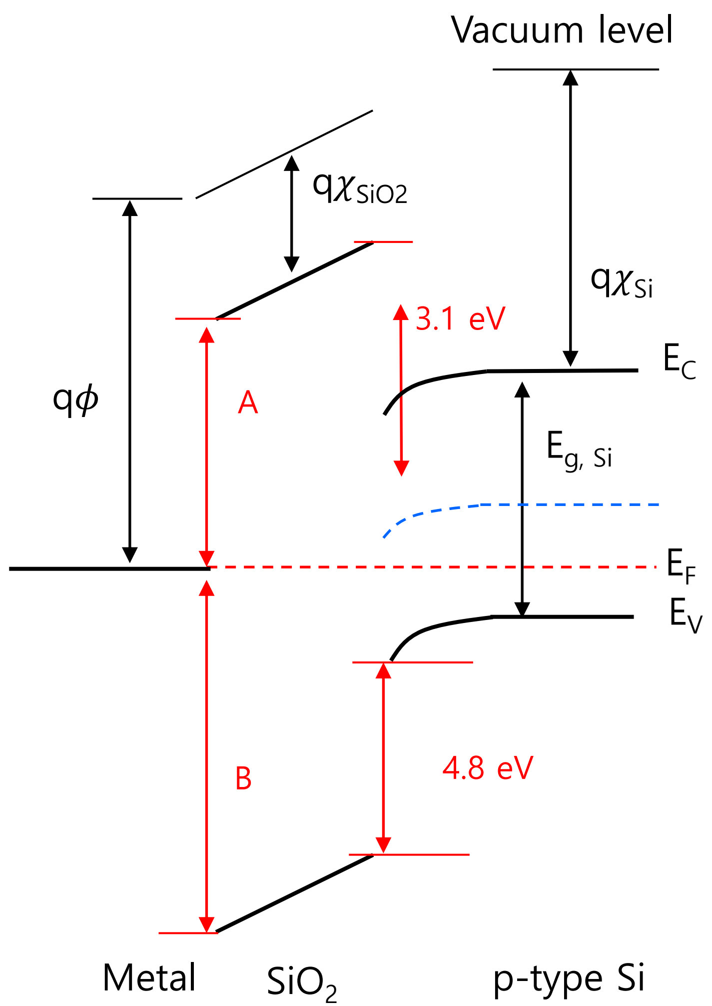


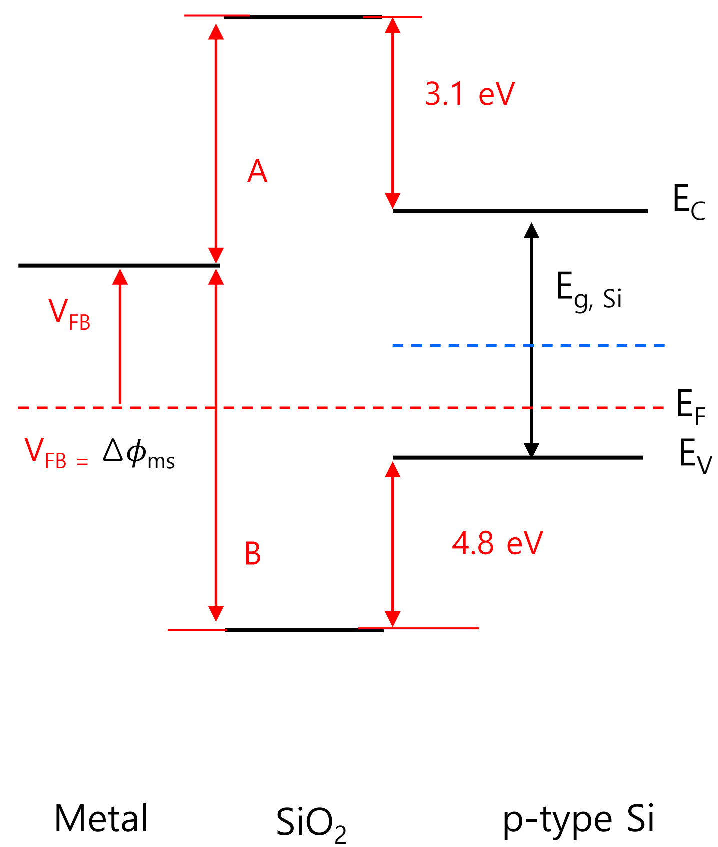
4. Principle of Semiconductor devices

Metal-Oxide-Semiconductor

1. Concept

: **Flat band voltage – the applied gate voltage such that there is no band bending in the semiconductor**





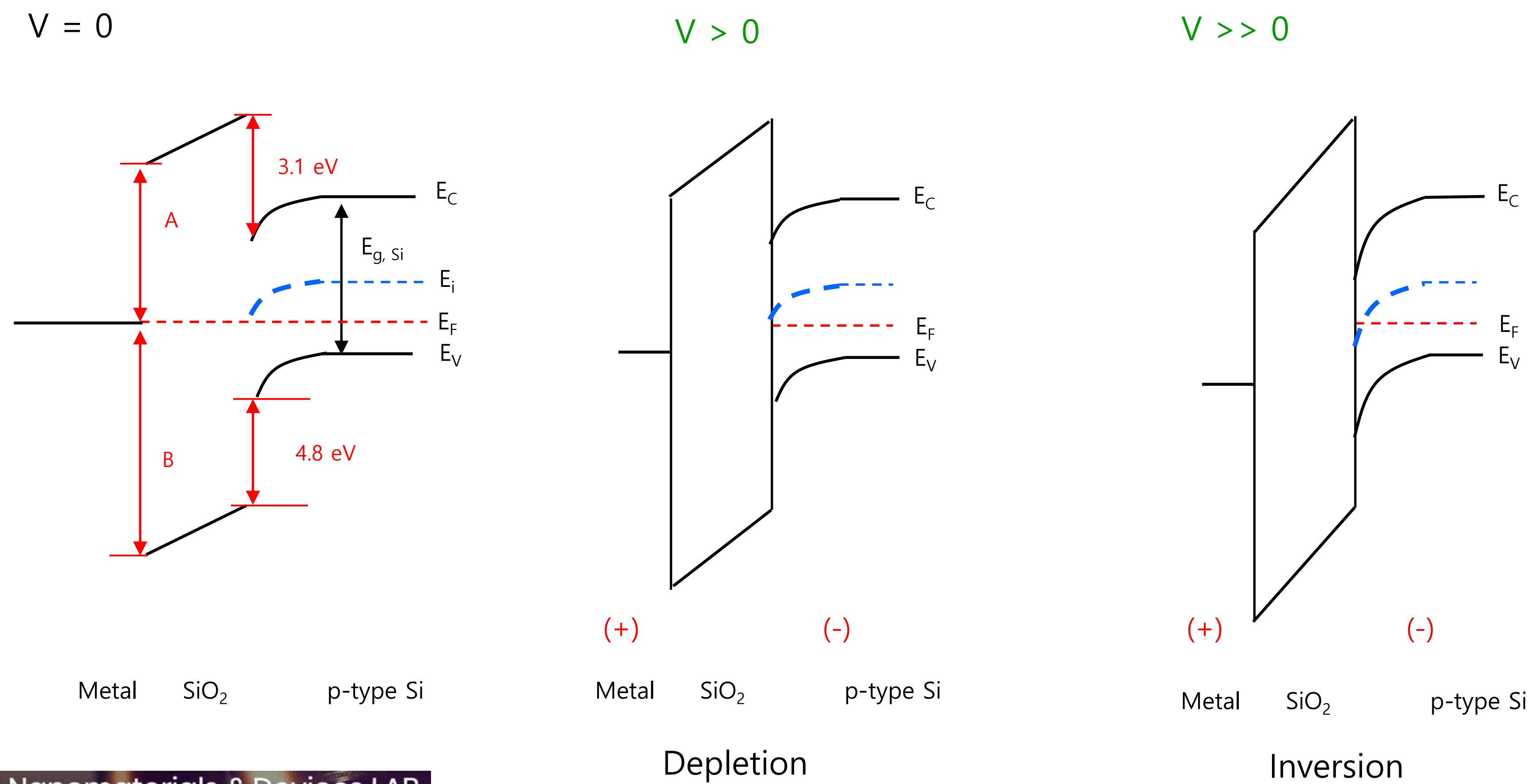
4. Principle of Semiconductor devices

Metal-Oxide-Semiconductor

1. Concept

: MOS capacitor structure

- **When, $\phi_m < \phi_{Si}$**

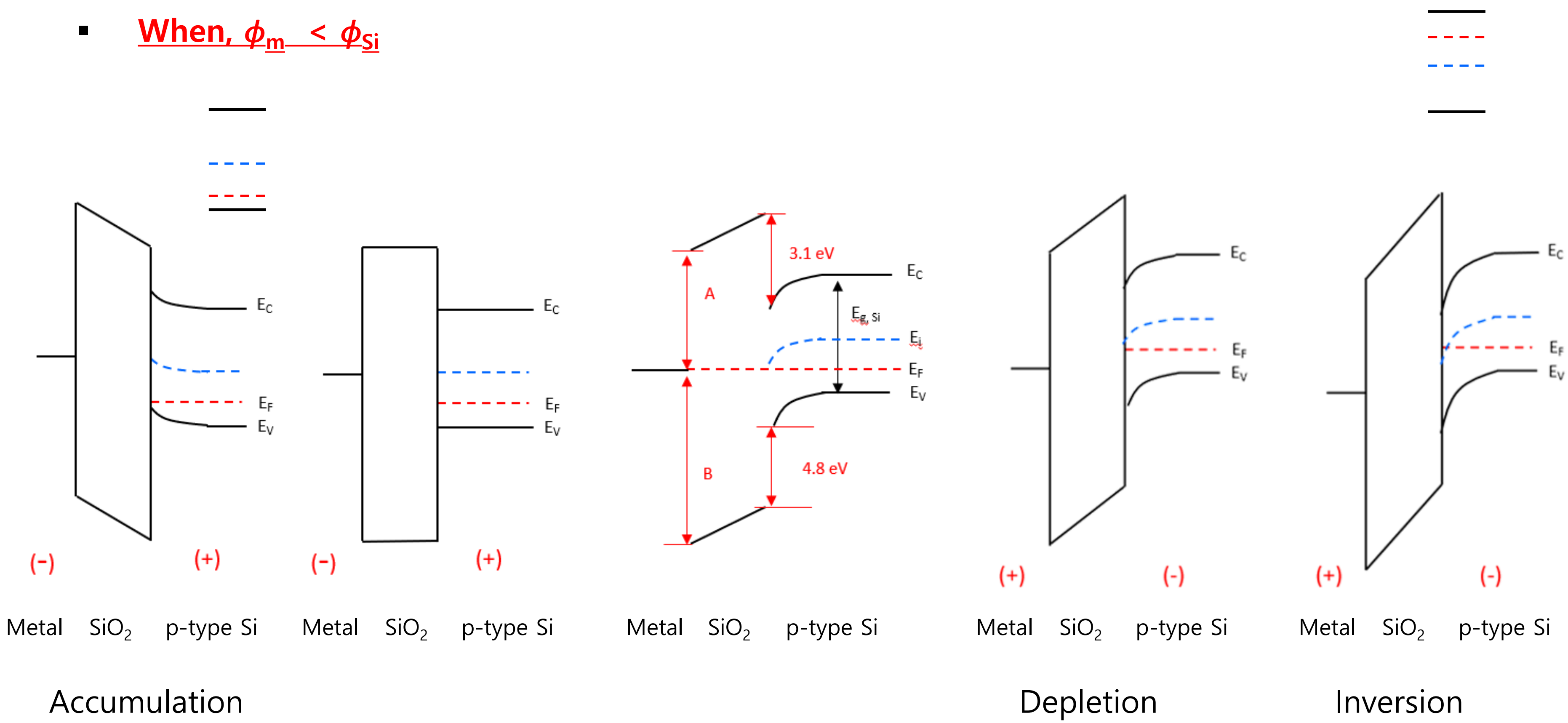


4. Principle of Semiconductor devices

Metal-Oxide-Semiconductor

1. Concept
: MOS capacitor structure

- **When, $\phi_m < \phi_{Si}$**



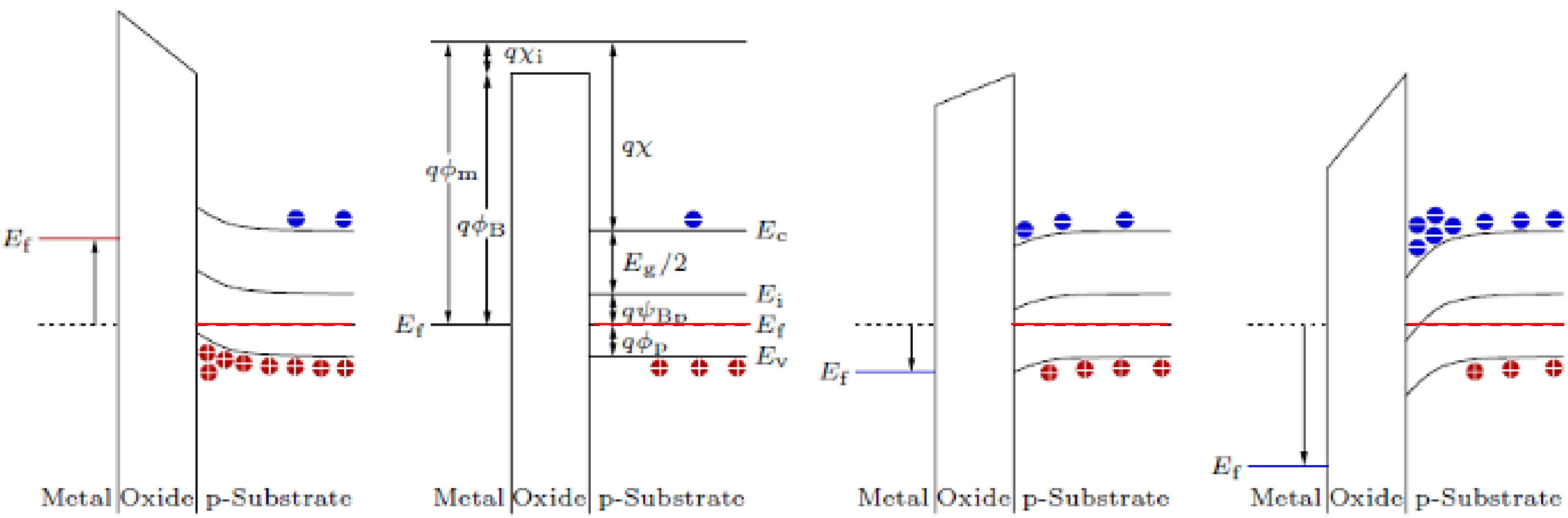
4. Principle of Semiconductor devices

Metal-Oxide-Semiconductor

1. Concept
: Operation modes

- **When, $\phi_m = \phi_{Si}$**

V << 0 | V_{FB} = V = 0 | V > 0 | V >> 0



(−) (+) | (−) (+) | (+) (−) | (+) (−)

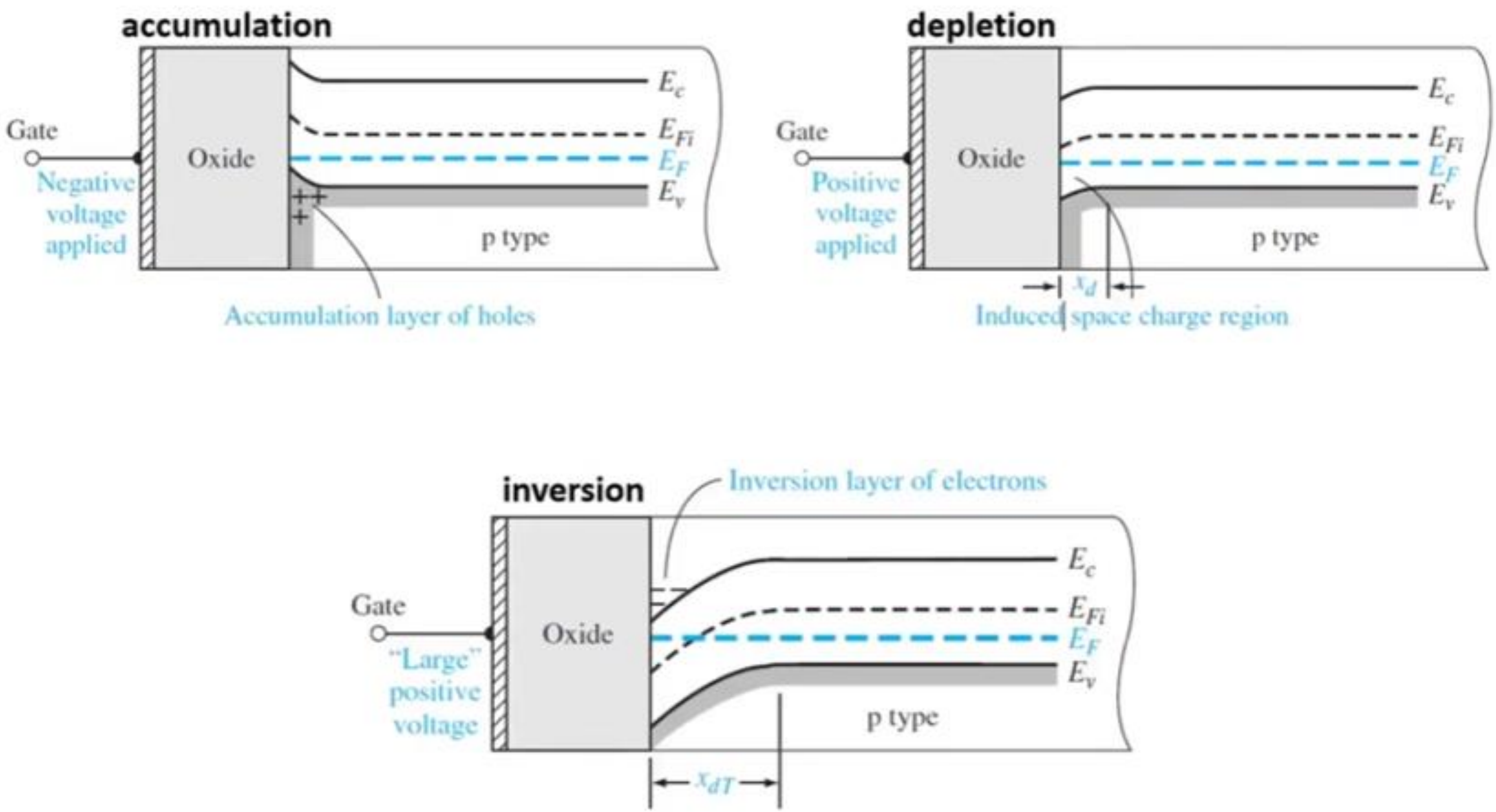
Accumulation | Flat band | Depletion | Inversion

4. Principle of Semiconductor devices

Metal-Oxide-Semiconductor

1. Concept
   : Operation modes

- When, $\phi_m > \phi_{Si}$

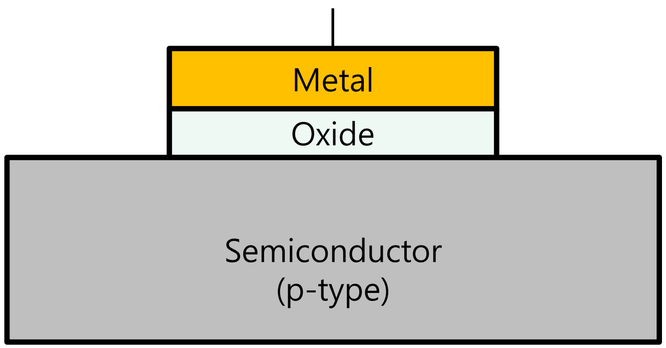


4. Principle of Semiconductor devices

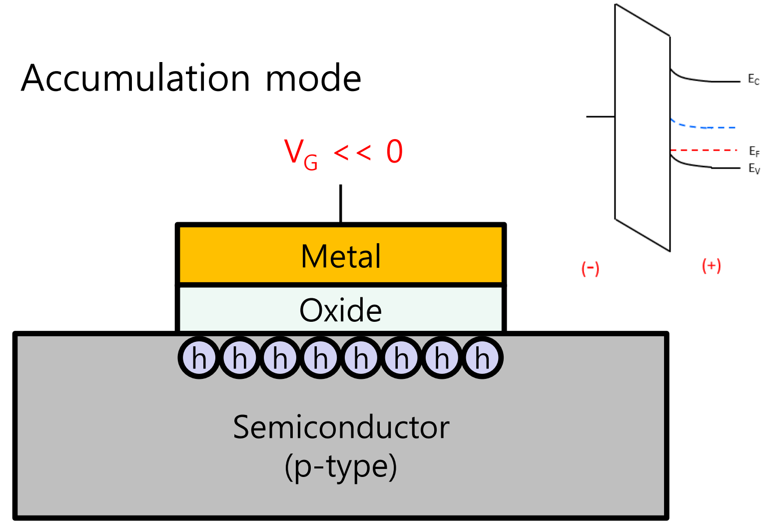
Metal-Oxide-Semiconductor

1. Concept
: Operation modes

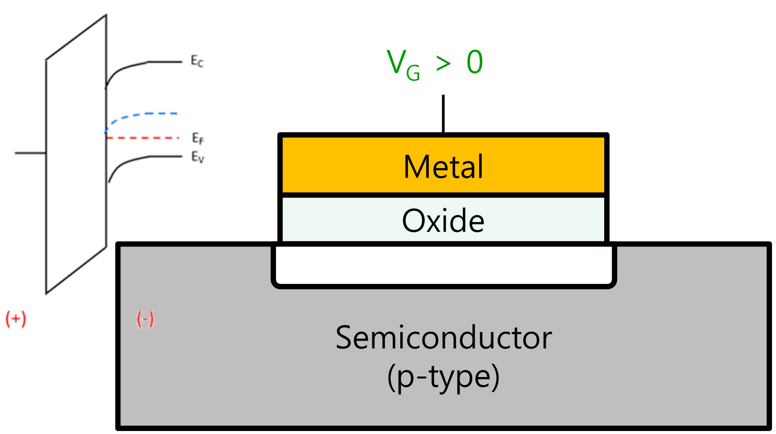
Non-base



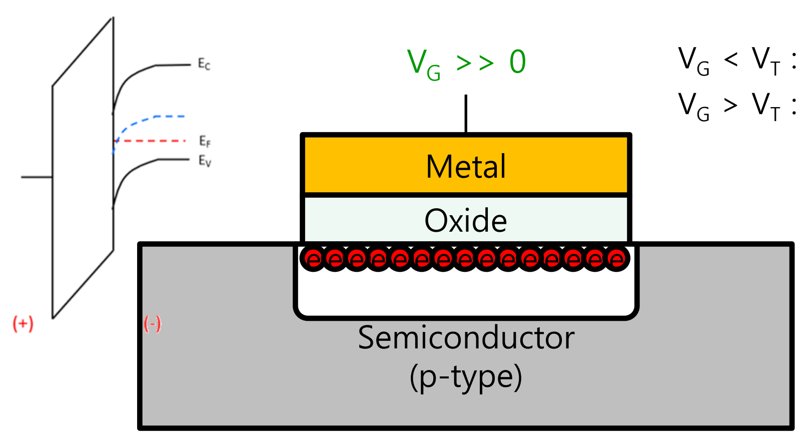
Accumulation mode



Depletion mode



Inversion mode



$V_G < V_T$: not inverted

$V_G > V_T$: inverted

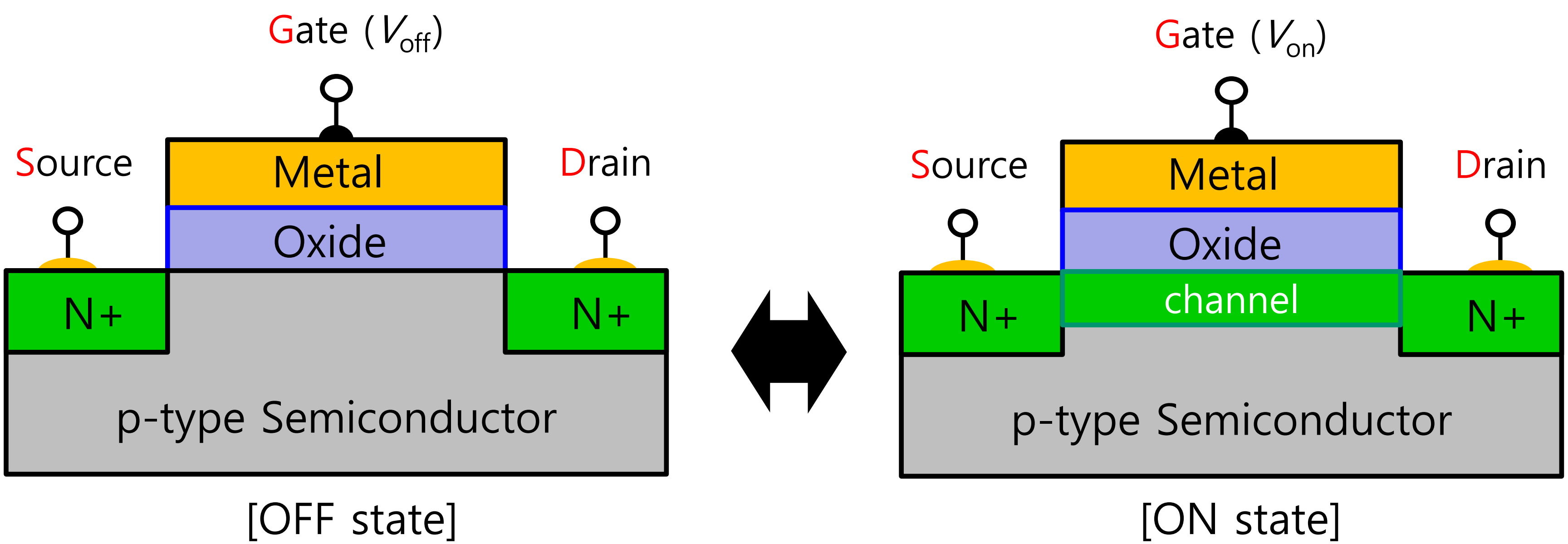
4. Principle of Semiconductor devices

Metal-Oxide-Semiconductor

2. MOSFET

How to switch the FET?

- Transistor is semiconductor device used to switch (or amplify) electronic signals and electric power using electric field.



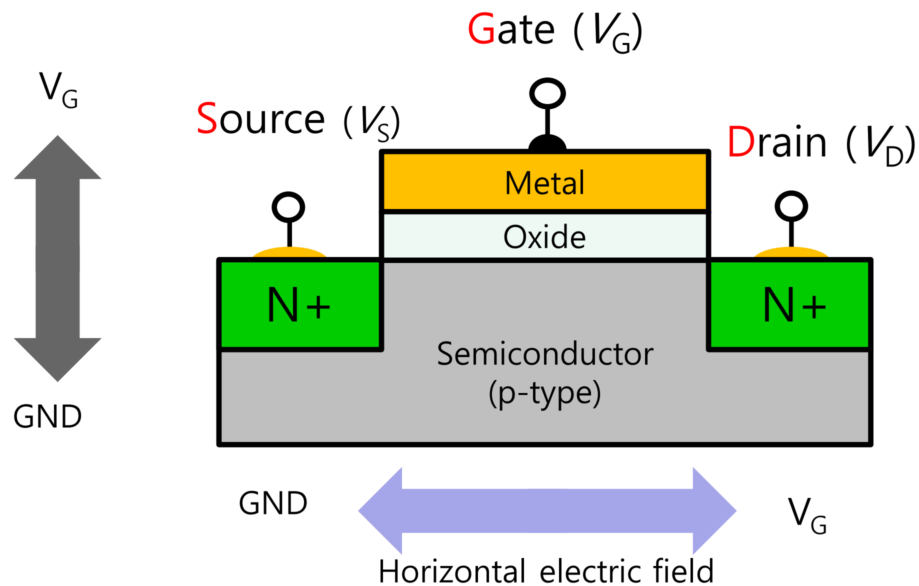
A: The gate controls the flow of current from the source to the drain electrodes by formation of channel

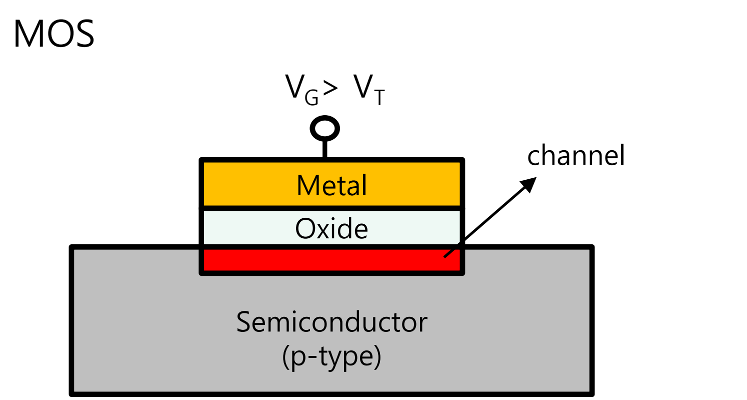
4. Principle of Semiconductor devices

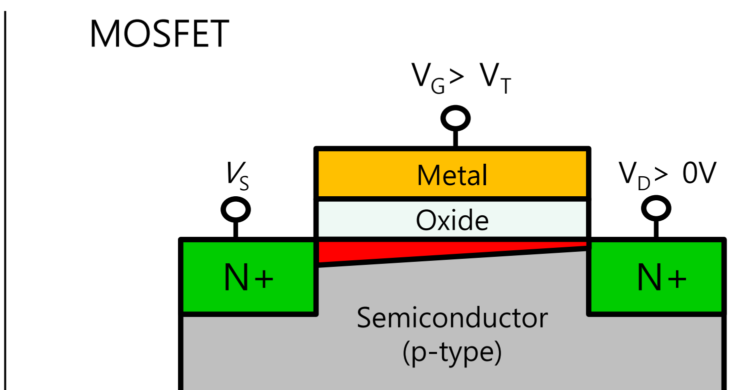
Metal-Oxide-Semiconductor

2. MOSFET

: electric field







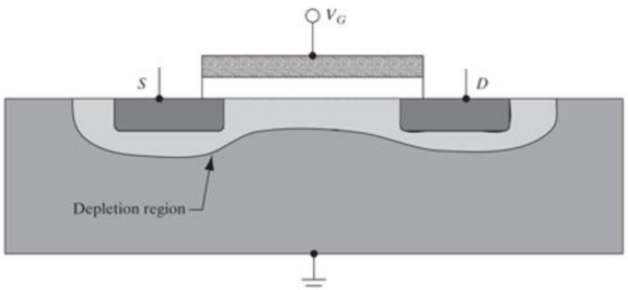
- Inversion channel is formed or not, depending on the interaction of V_{GS} and V_{GD}
- The depth of the formed channel varies depending on the location

4. Principle of Semiconductor devices

Metal-Oxide-Semiconductor

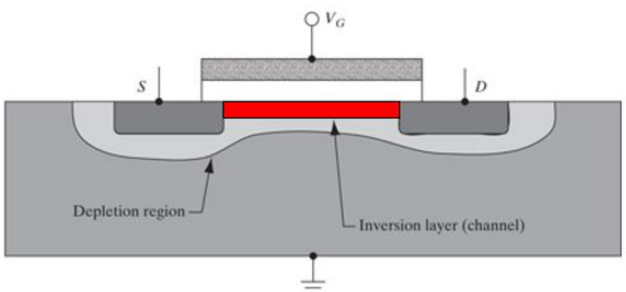
2. MOSFET

2-1. Operation process



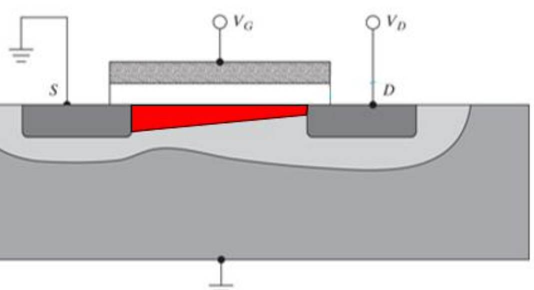
V_S = V_D = GND

$V_G < V_T$: accumulation or depletion state



V_S = V_D = GND

$V_G > V_T$: Inversion state



V_S = GND, low $V_D > 0V$

$V_{GS} > V_T$: Inversion state

$V_{GD} > V_T$: Inversions state

Channel is formed in all area between S/D

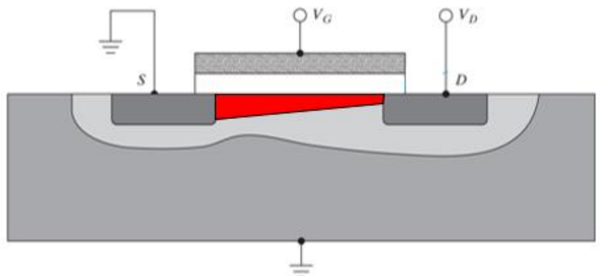
V_D ↑ > I_{DS} ↑ : Linear region

4. Principle of Semiconductor devices

Metal-Oxide-Semiconductor

2. MOSFET

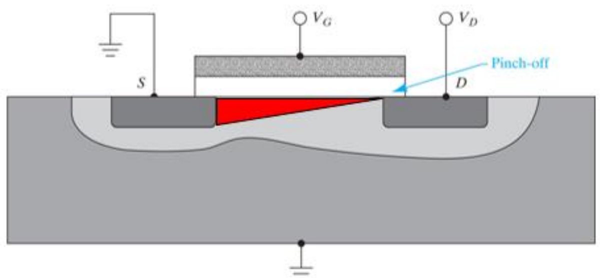
2-1. Operation process



V_S = GND, low V_D > 0V

V_{GS} > V_T : Inversion state

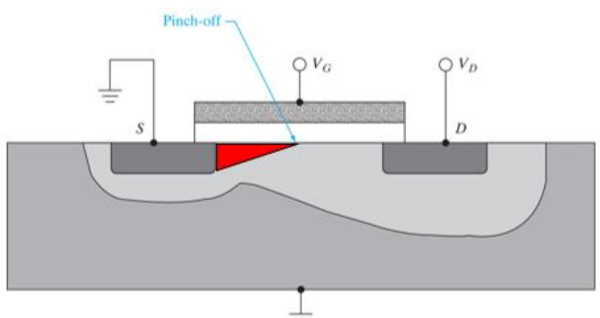
V_{GD} > V_T : Inversions state



V_S = GND, Mid. V_D > 0V = pinch off voltage

V_{GS} > V_T : Inversion state

V_{GD} = V_T : Pinch-off state



V_S = GND, High V_D > 0V

V_{GS} > V_T : Inversion state

V_{GD} > V_T : Depletion state

Channels is partially formed between S/D

V_D ↑ > maintain I_{DS} : Saturation region

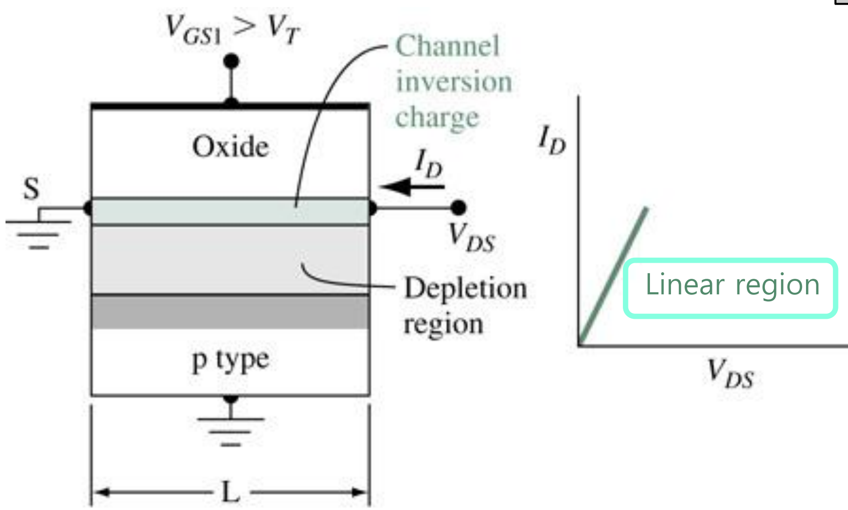
4. Principle of Semiconductor devices

Metal-Oxide-Semiconductor

2. MOSFET

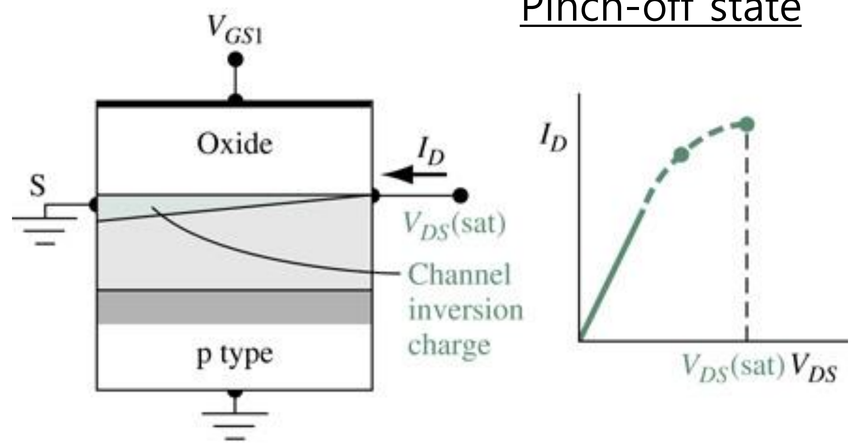
2-1. Operation process ($V_{GS} > V_T$: Inversion state)

i) low V_D

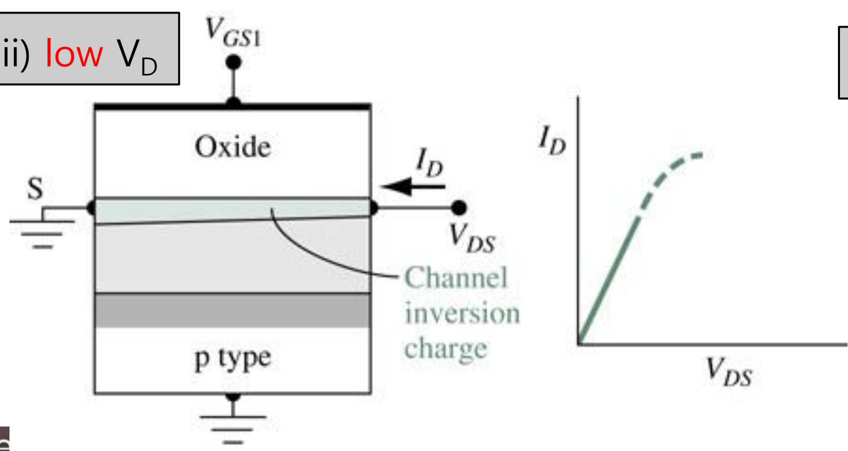


iii) pinch-off V_D

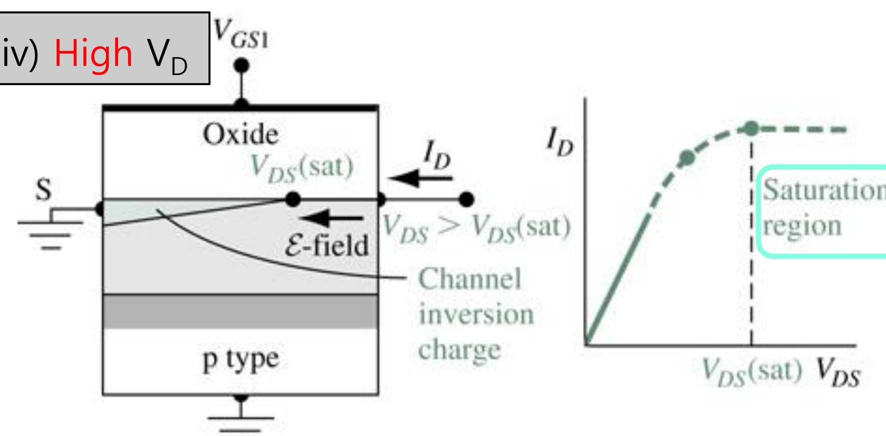
Pinch-off state



ii) low V_D



iv) High V_D



4. Principle of Semiconductor devices

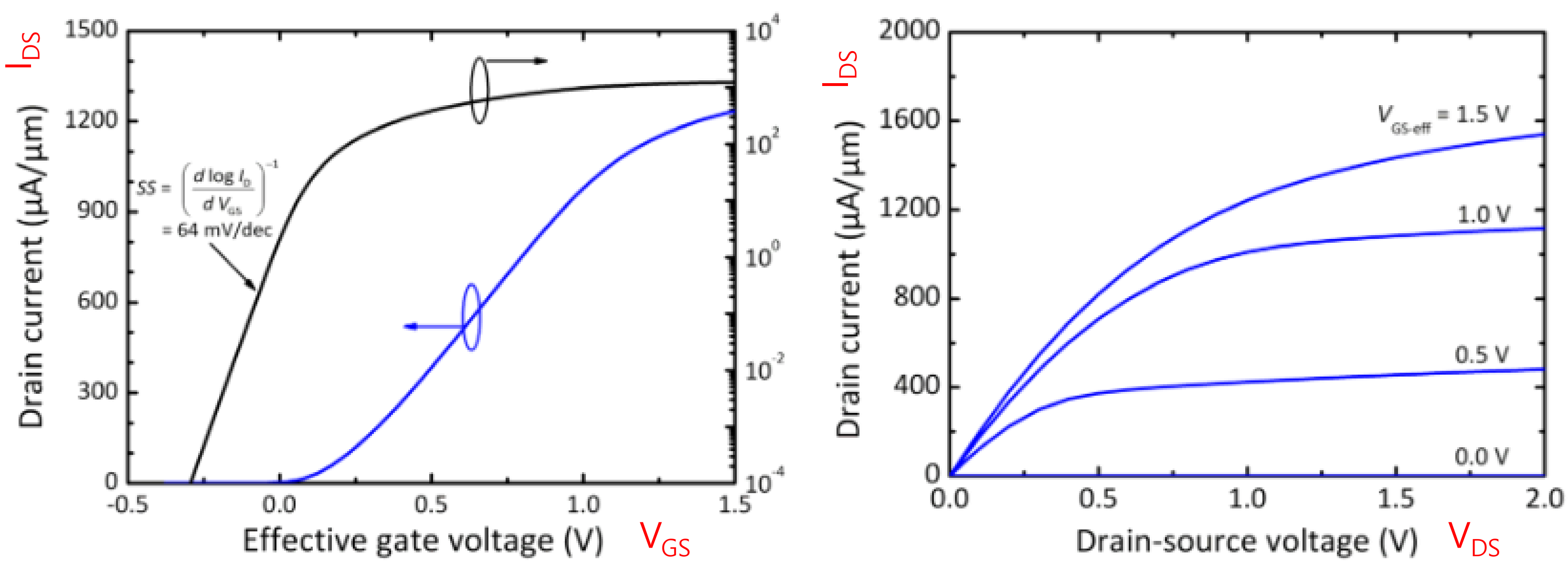
Metal-Oxide-Semiconductor

2. MOSFET

2-1. Operation process

: Output characteristic (V_{DS} – I_{DS} curve)

Figure 5. Steady-state characteristics of the simulated 50-nm gate single-channel GNR MOSFET: (**a**) transfer characteristics; and (**b**) output characteristics.



(a) (b)

4. Principle of Semiconductor devices

Metal-Oxide-Semiconductor

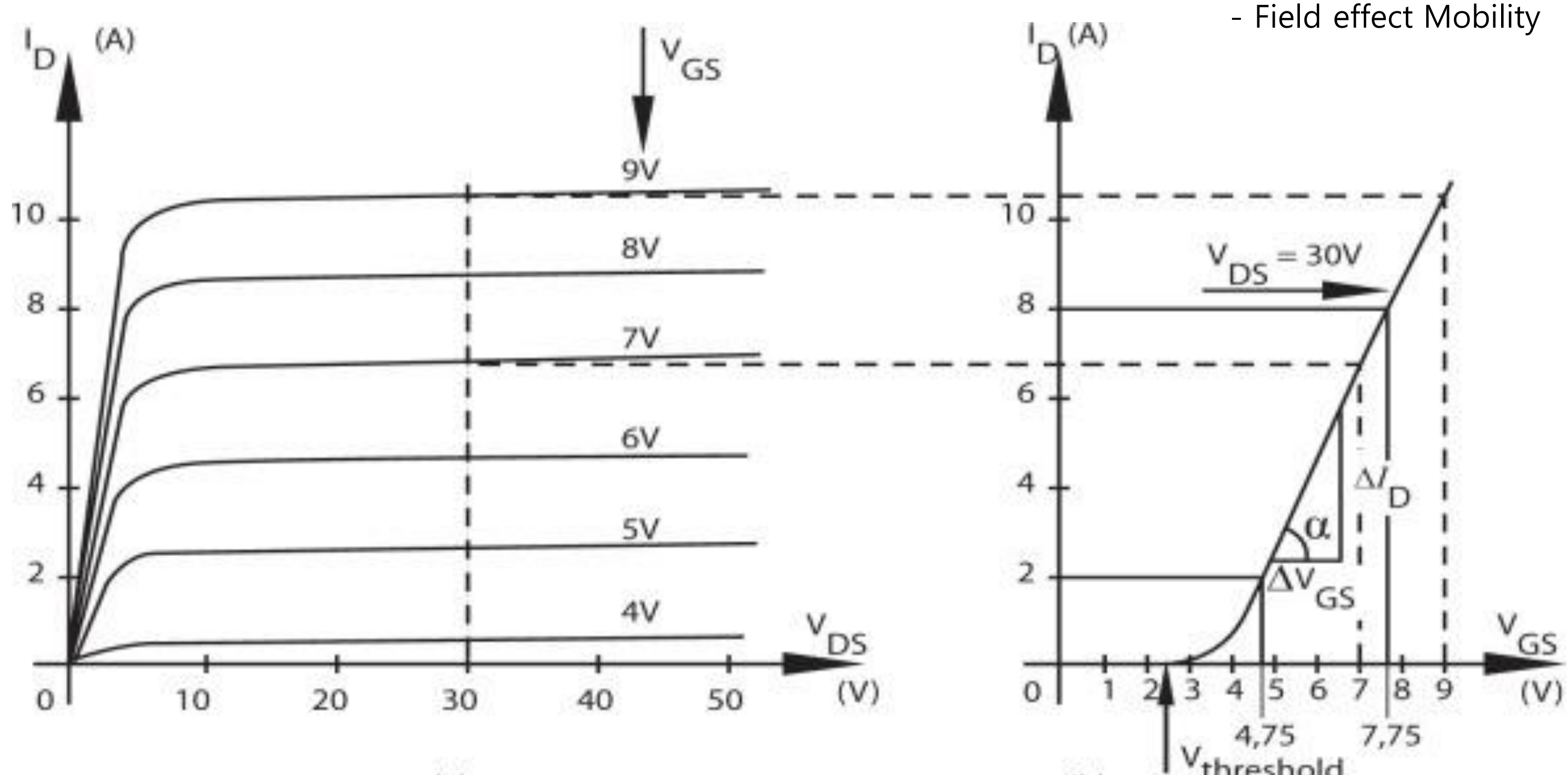
2. MOSFET

2-1. Operation process

: Transfer characteristic (V_{GS} – I_{DS} curve)

FET parameter

- Threshold voltage
- Subthreshold swing
- On/off ratio
- Field effect Mobility



(a) (b)

4. Principle of Semiconductor devices

Metal-Oxide-Semiconductor

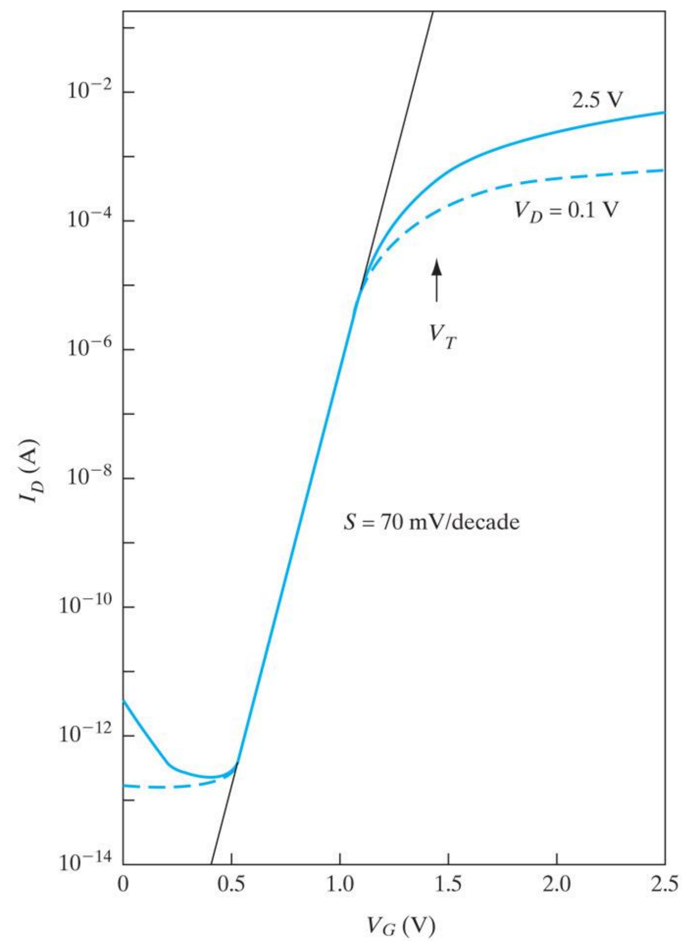
2. MOSFET

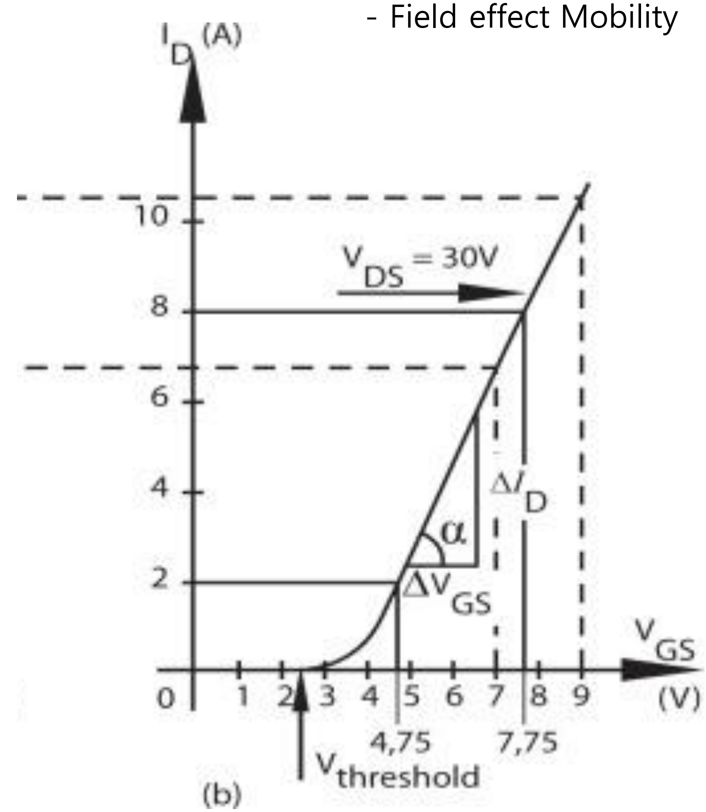
2-1. Operation process

: Transfer characteristitic (V_{GS} – I_{DS} curve)

FET parameter

- Threshold voltage
- Subthreshold swing
- On/off ratio
- Field effect Mobility





4. Principle of Semiconductor devices

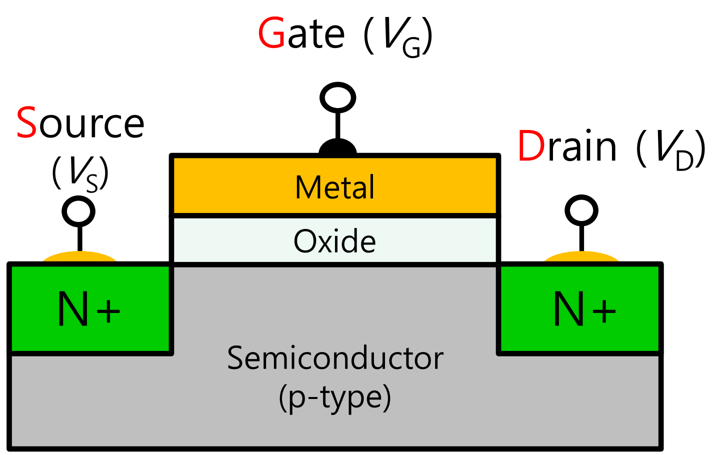
Metal-Oxide-Semiconductor

2. MOSFET

2-2. Types of MOSFET

Enhancement mode

: normally "OFF"

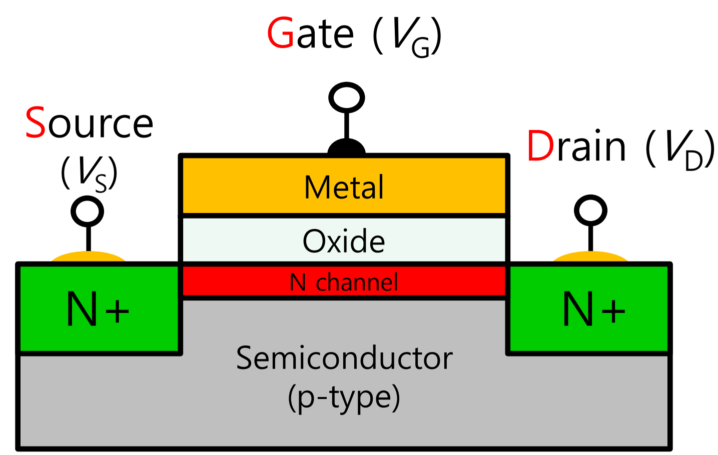


No channel when V_G = 0 V

Conductivity at channel area **is enhanced** by applying a gate voltage

Depletion mode

Normally "ON"



Channel when V_G = 0 V

Conductivity at channel area **is depleted** by applying a gate voltage

4. Principle of Semiconductor devices

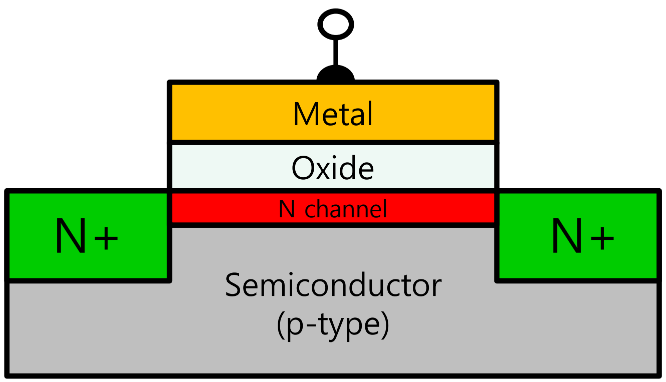
Metal-Oxide-Semiconductor

2. MOSFET

2-2. Types of MOSFET

N-channel MOSFET

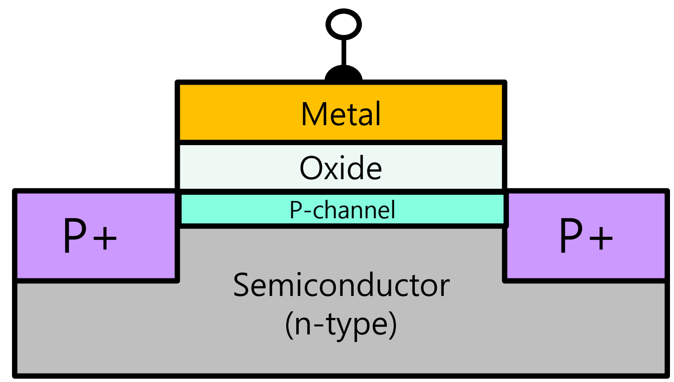
(NMOS)



$0V < V_T < V_{GS}$

P-channel MOSFET

(PMOS)



$V_{GS} < V_T < 0V$

NMOS & PMOS operate in a complementary manner

"CMOS" = Complementary MOS

for constructing integrated circuit (IC) chips, including microprocessors, microcontrollers, memory chips, and other digital logic circuits.

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